Highly conductive electrodes as diffusion barrier for high temperature applications

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Abstract

The semiconductor industry calls for the integration of high-κ materials (κ>100) in CMOS based chips as capacitor dielectric in DRAM cells. Another possible application of high-κ materials on silicon is in bioelectronics for capacitive stimulation of nerve cells for the investigation of the interaction between chip based circuits and living cells.
The most promising materials for this purpose are those with perovskite structure, such as $BaTiO_3$ (BTO) and $(Ba,Sr)TiO_3$ (BST). During the processing of perovskite materials at high temperatures (550-700 °C) and post annealing oxygen diffuses through the platinum grain boundaries and reacts with the underlying silicon plug. The formation of silicon dioxide (SiO_2) with a lower dielectric constant reduces the overall capacitance. The scope of this work was to develop a conductive oxygen diffusion barrier for the processing of high-κ materials (e.g. BST) on good conducting, highly p-doped silicon wafers ($p^{++}Si$) to be used as a bottom electrode in the metal-insulator-metal (MIM) thin film capacitor stack. Tantalum-silicon-nitride (TaSiN) is the one of the most promising materials for this application.
TaSiN was deposited using reactive rf-magnetron sputtering technique from $TaSi_x$-targets (x = 1 and 2.7) in a nitrogen atmosphere at room temperature and 500 °C. The cathode power and the nitrogen flow were varied in order to gain different $Ta_xSi_yN_z$ compositions. The film composition was determined using Rutherford backscattering spectroscopy. The sheet resistance of as-deposited films and after annealing at 700 °C was measured using a four point probe method. The as deposited films have metallic conduction with Ohmic behaviour. The room temperature resistivity of as deposited films with different compositions depends on the nitrogen content and is in the range from 10^{-6} Ωm up to 10^{-3} Ωm. The as deposited TaSiN films are amorphous. The crystallisation temperature of thin TaSiN films was defined as the temperature at which the crystalline $TaSi_2$ phase was formed as identified by XRD. For all composition it was found that the crystallisation temperature is above 700 °C and increases with higher nitrogen content.
It was found that an as-deposited $p^{++}Si$/TaSiN junction develops unacceptable contact resistance. Introducing an intermediate Pt layer (100 nm) the $p^{++}Si$/Pt/TaSiN stack showed a good conductive properties and good thermal stability at 700 °C. Above 500 °C the thin platinum layer reacted completely with the Si substrate forming conductive platinum-silicides (PtSi, Pt_2Si, Pt_3Si) as detected by X-ray diffraction. The deposition of high-κ material directly on the TaSiN surface and subsequent annealing in an oxygen atmosphere at 700 °C resulted in the reduction of the overall capacitance. An additional protective layer (platinum or iridium) improved the stack $p^{++}Si$/Pt/$Ta_{21}Si_{57}N_{21}$/Ir(Pt) behaviour after annealing at elevated temperature. But the roughness above 600 °C was unacceptably high. After annealing at 550 °C the stack Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir remained conductive. The roughness measured on the top layer was lower than 1 nm and acceptable for the further implementation. The BST layer was deposited using PLD at 550 °C on the Si/Pt/ $Ta_{21}Si_{57}N_{21}$/Ir stack. For the electrical measurement a top Pt layer was deposited by DC magnetron sputtering and structured by a lift-off lithographic process. In order to measure the whole stack, the bottom side of the $p^{++}Si$ wafer was coated with a 100 nm thick platinum layer and fixed with silver paste on a copper plate which served as a bottom electrode. The dielectric properties are promising: the dielectric constant at zero field is $\kappa \approx 470$ and gives a large advantage for the biological application compared to the dielectrics (TiO_2 or HfO_2) used in earlier research. The capacitance – el. field dependence has a slightly butterfly shape, indicating some ferroelectricity in the thin BST film, and the curve is largely tuneable. The leakage current is not completely symmetric due to the different top and bottom electrodes, platinum and $p^{++}Si$, respectively. The absolute current is below 10^{-6} A/cm^2 for fields lower than ± 200 kV/cm corresponding to an applied voltage of ± 2 V, which is reasonable for DRAM applications.

Contents

Used symbols and abbreviations

Symbols

A, A_0	Capacitor area, Amplitude
A_J	Membrane area
a	Sample length
C	Capacitance, Correction factor, Curie constant
c	Speed of light, Molar heat capacity
c_M	Membrane capacitance
c_{ox}, c_{sat}, c_{DL}, c_{IL}, c_{acc}	Capacitance density of insulated oxide, total saturation, electrical double layer, interfacial layer and accumulation layer
d	Thickness, Sample width
d_{hkl}, d_J	Distance between crystal planes, Gap distance
e	Elementary charge
E	Electric field, Energy
E_{AC}	Small signal excitation field
E_F, E_G	Fermi energy, Bandgap energy
E_c	Minimum energy of conduction band
E_v	Maximum energy of valence band
f, f_α	Frequency, Atomic scattering factor
F	Correction factor for resistance calculation with for point probe
$\vec{G}_{hkl}$	Reciprocal lattice vector
g_K	Specific potassium conductance of the attached membrane
(hkl)	Miller indices
I, I_{cap}, I_L, I_{pip} ,I_{trans}	Current, Capacitive, leakage, pipette and transient current
I_K, I_P	Current through potassium (K^+) channels and pores
J	Current density
K	Kinematic factor
k_B	Boltzmann constant
k_0, k_{eff}	Initial spring constant, Effective spring constant
L	Absorption length
M	Atomic mass
N_A, N_B	Areal density of atom A and B in thin film

N_a	Acceptor concentration
N_v	Effective density of states in the valence band
n_{mol}	Molar density
P, P_S	Electrical polarisation, Spontaneous electrical polarisation
P_r	Remanent polarisation
P_{r+}, P_{r-}	Positive remanent polarisation, Negative remanent polarisation
P_{rrel+}, P_{rrel-}	Positive relaxed remanent polarisation, Negative relaxed remanent polarisation
$\vec{r}$	Space vector
R, R_S	Resistance, Sheet resistance
R_q, R_a	Root mean square roughness, Average roughness
s, S	Sample length, Energy loss factor
t	Time
t, t_{ox}, t_{phys}	Thickness, Oxide equivalent thickness, Physical thickness
T, T_C, T_0	Temperature, Curie temperature, Phase transition temperature
U	Voltage
V, V_C	Voltage, Coercive voltage
V_{C+}, V_{C-}	Positive coercive voltage, Negative coercive voltage
V_r, V_{in}, V_{out}	Resting potential, Potential inside and outside the cell
V_J, V_M,	Extracellular potential, Intracellular potential
V_S, $V_X{}^0$	Stimulation voltage, Reversal potential
w	Thickness
z, Z	Valence, Impedance

Greek symbols

α	Absorption coefficient
δ	Pulse duration
ε, ε_0, ε_r	Permittivity, Vacuum permittivity, Relative permittivity
θ	Incident angle
κ	Dielectric constant
λ	Wave length
ρ, ρ_J	Resistivity, Electrolyte resistivity
Φ	Work function

χ, χ_e	Electron affinity, Dielectric susceptibility

Acronyms

AC	Alternate current
AFM	Atomic force microscopy
ALD	Atomic layer deposition
BE	Bottom electrode
BST	Barium strontium titanate $(Ba_{1-x}, Sr_x)TiO_3$
BTO	Barium titanate $BaTiO_3$
C-V, C-E	Capacitance vs. voltage, Capacitance vs. electric field
CMOS	Complementary metal-oxide semiconductor
CSD	Chemical solution deposition
CVD	Chemical vapour deposition
DC	Direct current
DRAM	Dynamic random access memory
EOS	Electrolyte-oxide-silicon
GIXRD	Glancing incident X-ray diffraction
MIM	Metal-insulator-metal
ONO	Oxide-nitride-oxide
PLD, PLA	Pulsed laser deposition, Pulsed laser ablation
PVD	Physical vapour deposition
P-V, P-E	Polarisation vs. voltage, Polarisation vs. electric field
RBS	Rutherford backscattering spectroscopy
RTA	Rapid thermal annealing
SEM	Scanning electron microscopy
STO	Strontium titanate $SrTiO_3$
TE	Top electrode
XRD	X-ray diffraction
XRF	X-ray fluorescence

1 Introduction to the integration of highly conductive electrodes

The development of microelectronics in the last 25 years has been characterized by an exponential increase of the capacitance density in integrated circuits (ICs) with time. Such an evolution has been so regular as to deserve the name law – Moore's law, from the name of the person who first observed the trend [1]. Higher capacitance density can be achieved by the use of: 1) complex electrode structures providing a large surface area within a small lateral area, 2) thinner capacitors dielectrics, and 3) higher permittivity capacitor dielectric materials [2]. Remarkable increase in density has been brought about by advances in various areas of technology, including lithography, dry pattering, and thin film deposition technique. In general, increasing the surface area leads to increased complexity and hence increased cost. There are also the limitations on the dielectric thickness of conventionally used SiO_2 and SiN_x.

Much work in recent years has focused on the development of high-permittivity materials for dynamic random access memory (DRAM) capacitor. DRAM chips manufactured to date contain primarily capacitors utilizing a thin dielectric consisting of a mixture of silicon dioxide and silicon nitride sandwiched between two electrodes made of doped crystalline silicon or polycrystalline silicon.

Barium strontium titanate, $(Ba,Sr)TiO_3$ (BST), thin films have received a great deal of attention as likely candidates for DRAM applications. In the capacitor fabrication process, the BST thin films require a high temperature annealing of more than 550 °C in an oxidizing ambient during the deposition and/or post processing, independent of deposition process, in order to form the perovskite structure and thus the high permittivity. Most integration schemes for perovskite dielectrics use noble metal electrodes (platinum or iridium) as bottom and top electrodes. During the deposition of dielectric material or post annealing process

oxygen diffuses freely through bottom electrode grain boundaries and may oxidize the poly-silicon plug [3-4]. At temperatures below about 0.7*Tm* (in the case of platinum below 1238 °C) the contribution of the grain boundary diffusion becomes dominant [5]. Therefore there is a need to introduce an oxygen diffusion barrier at the electrode/poly-silicon plug interface to prevent the silicon oxidation.

Table 1.1 *Candidate materials which can be used as electrodes for BST and other high-permittivity dielectrics. Preparation methods, permeability to oxygen, and suitability for pattering into small features are indicated [2].*

Electrode material	Deposition methods	Oxygen permeability
Pt	PVD, CVD	High
Ir	PVD	Moderate

Table 1.1 lists materials potentially suitable for use as electrodes with BST and perovskite dielectrics, along with some of their relevant properties. The choice of electrode and barrier materials is very important for both processing and integration. The diffusion barrier must prevent plug oxidation and electrode/plug reactions and must remain conductive after the deposition and processing of the BST dielectric. The degree of oxidation resistance and oxygen diffusion-barrier function required for the diffusion-barrier material clearly depends on the severity of the oxygen exposure associated with the deposition and post-electrode anneals of the BST capacitor.

The choice of stacked-capacitor structure is also a factor. In a simple stacked-capacitor structure, the side of the barrier is directly exposed to the oxygen processing ambient [6]. Where the side of the barrier is covered with an insulating or noble-metal layer, the barrier is primarily exposed to oxygen diffusing through the electrode grain boundaries [7].

The oxidation resistance of the barrier material also depends on the properties of the barrier-material oxide that is formed. Some oxidation may be tolerable if the barrier oxide is not too resistive, but oxidation through the entire thickness of the barrier indicates that the barrier is not protecting underlying structures from exposure to oxygen. Finally, the demands on the barrier material also depend on the choice of the electrode. For example, an oxygen-permeable electrode material such as Pt would require a more oxidation resistant barrier then the less oxygen-permeable electrode material Ir.

Another key requirement for the barrier material is that it prevents diffusion of plug material and/or silicon into the electrode. This is particularly important for plug materials of

potentially "silicon contributing" materials such as doped polycrystalline Si, which can react with noble-metal electrodes to form noble-metal silicides. In addition to forming a silicide, silicon can also diffuse to the electrode surface to form SiO_2 layer which will lower the overall capacitance. These various barrier failure modes are illustrated in Figure 1.1.

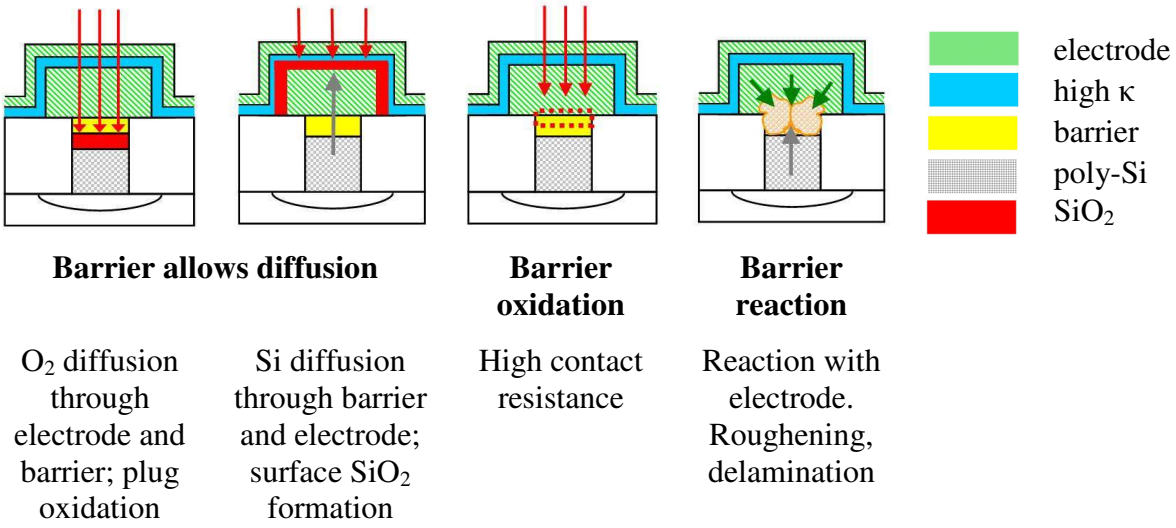


Figure 1.1 *Schematic representation showing the possible failure modes of the barrier during thermal processing in an oxidizing ambient [2].*

Some representative barrier materials are listed in Table 1.2 and consist mostly of various metal nitrides and metal silicon nitrides. Barriers used with doped polycrystalline Si plugs typically include a metal silicide layer at the barrier/plug interface to lower contact resistance (for example, the silicide $TiSi_2$ with barrier TiN).

Table 1.2 *Candidate materials which can be used as a barrier layer between the lower electrode and the conducting plug in stacked-capacitor DRAM structure with BST dielectric layer. These films can all be produced by reactive ion sputtering.*

Barrier material	Processability	Resistivity, [mΩcm]	Oxidation resistance
TiN	Easy	0.2	Poor
TaN	Easy	0.3	Poor
TiAlN, TaAlN	Moderate	0.4	Good
TaSiN	Easy	1-10	Excellent

Tantalum silicon nitride (TaSiN) is regarded as one of the more promising barrier materials [8, 9]. Unlike the other barrier materials listed in Table 1.2, TaSiN remains amorphous (and

thus free of fast diffusion path grain boundaries) over a wide range of compositions [10]. Depending on the exact application, the TaSiN composition can be optimized for oxidation resistance, barrier properties, or low resistance. Increasing film nitrogen content typically improves Si diffusion barrier performance but lowers conductivity, and decreasing Ta content typically improves barrier oxidation resistance. The performance of TaSiN as barrier layer for copper (Cu) interconnections is effective for the films that contain more then 51 % nitrogen and show no electrical degradation after annealing at 500 °C for an hour in Si/Cu metallization [11].

1.1 Dynamic Random Access Memory (DRAM)

1.1.1 Principle and limitation

The DRAM cells consist of two basic elements: the access transistor, which is addressed through a word line connected to the gate, and a capacitor, where the information is stored in form of electric charge. A schematic 1-bit cell is illustrated in Figure 1.2. As soon as the word line is connected to the operation voltage, the transistor switches to the operation state. The capacitor can then be accessed through the bit line and can be alternated/written with a zero-level voltage (logical "O") or the operating voltage (logical "1"). Relative to the bottom electrode, which is permanently connected to a *Vcc*/2 voltage, the capacitor will be charged with a half negative ("O") or half positive ("1") operation voltage, respectively. After the writing sequence the transistor is deactivated. Since the capacitor is not ideal, the voltage across the capacitor plates drops due to self discharge (leakage). This is why the information has to be periodically renewed in regular intervals also known as refresh intervals. According to the JEDEC (Joint Electron Device Engineering Council) standard DRAM cell must keep its information for a minimum time of 64 ms [12].

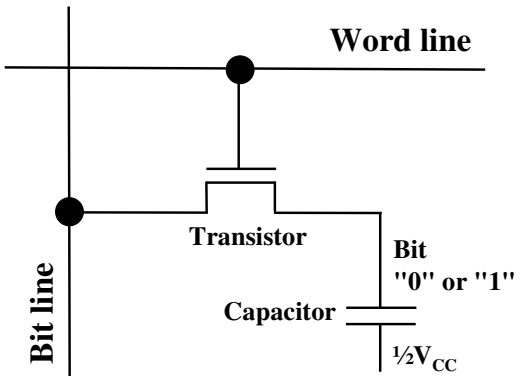


Figure 1.2 *Schematic representation of a 1T-1C DRAM cell.*

The read out of the stored information is initiated by pre-charging the bit line and a reference line with *Vcc*/2. The access transistor is then activated, so that the charge in the cell capacitor flows in the parasitic bit line capacitance. This charge relocation causes a slight rise or sinking of the voltage over the bit line. The sense amplifier compares this voltage with a reference value and then interprets the difference as a logical "1" or "O". In a real memory chip the parasitic capacitance is much higher then the cell capacitance. As a result, the signal level of the voltage difference is very low (100 mV – 200 mV) which makes the read out process more difficult. The read out of a DRAM is a destructive operation, so that the capacitor always has to be recharged (re-written) after reading.

Since the evolution of the sense amplifiers is rather expensive, the minimum charge in the cell capacitor can not be reduced along with the on-going miniaturization of the cell dimensions.

The capacitance *C* of a planar capacitor is given by the equitation:

$$C = \varepsilon_0 \varepsilon_r \frac{A}{t} \qquad (1.1)$$

where *A* is the surface of the electrode, *t* thickness, ε_0 and ε_r represent the dielectric constant of the vacuum and the relative dielectric constant of the dielectric material. Hence, the capacitance per area (the capacitance density) on chip could be increased by reducing the thickness of the dielectric, increasing the dielectric constant and increasing the active area by 3-dimensional capacitor structures.

The initially used SiO_2 dielectric has been replaced by oxide-nitride-oxide (ONO) coatings consisting of a $SiO_2/Si_3N_4/SiO_2$ stack almost since the very beginning of the DRAM technology, since they offer a higher dielectric constant (approximately 7 compared to 3.9 for pure SiO_2) plus some additional advantages regarding defect passivation and layer

planarization [13]. Nevertheless, SiO_2 remains the reference material for the comparison of the merits of new materials in terms of the oxide equivalent thickness t_{ox}^{eq}. This value describes the necessary thickness of a fictive SiO_2 layer in the same geometry in order to achieve the same charge densities as a high-k material and is defined as follows:

$$t_{ox}^{eq} = \frac{\varepsilon_{SiO_2}}{\varepsilon_r} t_{phy} \tag{1.2}$$

Equation (1.2) is based on the capacitance formula (1.1); t_{phy} represents the physical thickness of the high-κ dielectric, while ε_{SiO_2} and ε_r are the relative dielectric constants of the silicon dioxide and high-κ material, respectively.

The DRAM development has led to a quadrupling of the memory density on a single chip every 3 years [14]. Additionally, the on-going miniaturization has reduced the cell size by a factor of 18.8 in the time between the 4 Mb and the 256 Mb generations due to major improvements in lithography and innovative processing. In recent years there has been a shift from a technology generation strategy (4 Mb / 0.7 µm, 16 Mb / 0.5 µm, etc.) to a shrink strategy (64 Mb / 0.35 µm / 0.25 µm / 0.2 µm, etc.) with shorter development cycle. As the detection limit of state of the art sense amplifier lies at 20 to 30 fC/cell, the minimum charge of the 1T-1C cell capacitor was quickly reached for the planar designed along with a shrinking of dimensions even after reducing the capacitor's thickness to a minimum [15]. The following generations of DRAMs emerged the manufacturing of 3D capacitors in form of a stacked or a trenched cell. In the 64 Mb generation the stacked cell 0.25 µm minimum feature size required cylindrical capacitor with around 1 µm height and a trench cell with the same design rule required ~ 7 – 8 µm depth of trench, respectively [16]. Further shrinking of the cell capacitor is translated into more complex processing in terms of deeper trenches or more complex 3D structures, which complicate wafer processing and cause increasing manufacturing costs. Figure 1.3 represents the IBM concept of 64 Mb capacitor. The trench capacitors have depth more than 7 µm and width 250 nm resulting in an aspect ratio (depth/width) of near 30. In 2001 a new milestone in the DRAM density is reached by Samsung. Samsung presented 4 Gb chip on 0.10 µm CMOS (complementary metal–oxide–semiconductor) process with stacked capacitor cell using Ta_2O_5 ($\varepsilon_r \sim 25$) as capacitor dielectric [17].

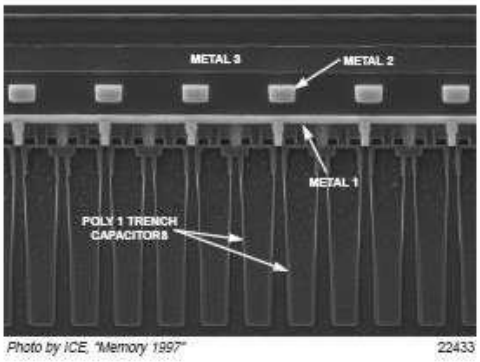


Figure 1.3 *IBM 64Mb deep trench capacitors.*

The ONO dielectric has a dielectric constant around 7.0, which requires an oxide-equivalent thickness around 4.5 – 5.0 nm and the thickness limit of ONO dielectric is considered to be around 3.5 – 4 nm in oxide equivalent thickness. Below this point, the rapid increase of the tunneling leakage current, that reduces the capacitors charge to unacceptable levels, can not be avoided [13]. Hence, the ONO trench or stack cell are no longer appropriate for the multi-gigabit density DRAMs and the SIA (Semiconductor Industry Association) roadmap considers the introductions of new high-κ materials [14].

1.1.2 High-κ materials processing

In terms of new DRAM technology the interesting materials are with dielectric constant larger than ONO. This has resulted in introduction of dielectric materials, such as aluminium-oxide (Al_2O_3), hafnium-oxide (HfO_2) and tantalum-oxide (Ta_2O_5), and potentially discussed material is BST. Table 1.3 summarizes some data from a recent near term SIA roadmap for stacked capacitors. It is obvious that multi Gbit DRAMs can no longer be manufactured by conventional technology, since the theoretical oxide equivalent thickness for these devices would be smaller then the lattice constant of the oxide.

In case the DRAM concept remains unchanged in the following generation, high-κ materials such as BST will be needed in order to achieve the necessary equivalent oxide thickness for the capacitor cells, even though the requirements of higher retention times, e.g. 64 ms for 0.07 μm generation and low temperature processing (< 500 °C), will be a great and difficult challenge for BST dielectric. IBM has preformed an advanced study in the integration of BST in form of a stacked capacitor in an attempt to examine the possibilities and prospects of using „exotic" materials [2].

Table 1.3 *The roadmap for DRAM Technology (source SIA [18]).*

ITRS Technology Nodes and Chip Capabilities			
Year	2009	2010	2014
DRAM Half-Pitch, [nm]	50	45	30
Equivalent oxide thickness (EOT), [nm]	0.80	0.60	0.30
Microprocessor Physical Gate Length, [nm]	20	18	13
Dielectric constant	48.75	65	98
Microprocessor Speed, [Hz]	5.5	5.9	7.9

The feasibility of a BST cell using a 0.2 μm design rule, Pt electrodes and TaSiN barriers in a simple stacked structure was demonstrated. The IBM design approach is presented in Figure 1.4 along with the major problems that arise from the introduction of new materials and additional processing. The electrode aspect ratio of ~ 1.2 that can be derived from the Transmission Electron Microscopy (TEM) figure and the BST film thickness of 27 nm meet the requirements for the 1 Gbit generation.

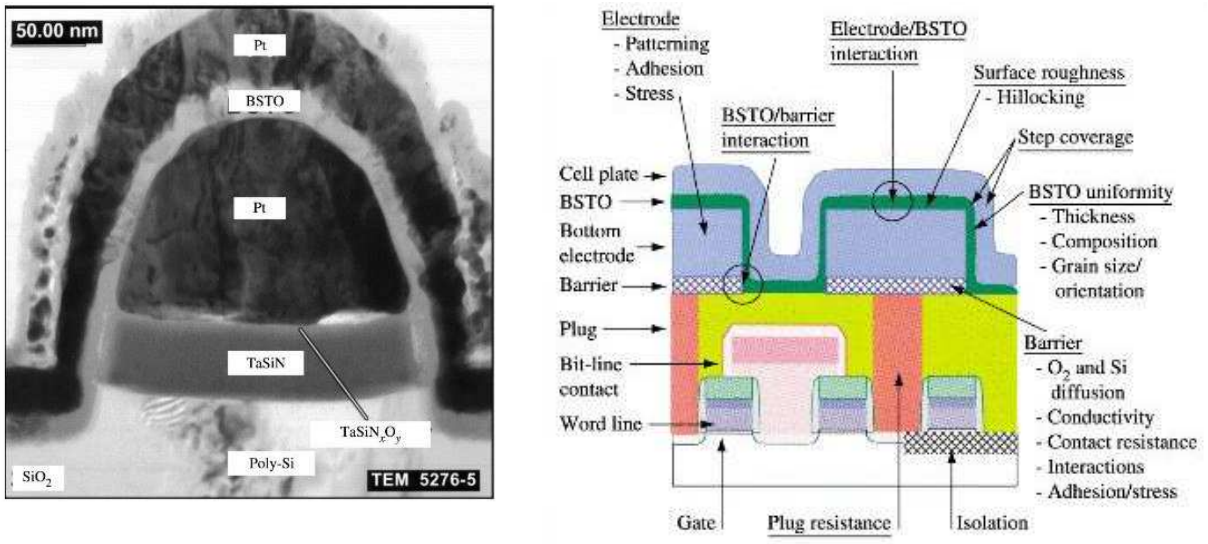


Figure 1.4 *a) Cross section TEM of a prototype Pt/BST/Pt capacitor b) Major concerns for the integration of the BST dielectric [2].*

Not only the high permittivity and the typical integration requirements, like compatibility with the standard methods, but also a large number of additional requirements have to be fulfilled in order to accept a new material in the closed family of the silicon industry. The diversity of the integration problems of high-κ materials has driven many serious research efforts worldwide [2, 19-22].

In the Table 1.4 one may find the most important requirements for the thin film dielectric to be introduced in the Gbit generation. The second column indicates whether there is primarily a process (P) or material (M) requirement. Although most of the requirements may be considered as twofold, depending on both material and processing parameters, many of the problems are closely related to processing issues and this work aims to investigate some aspects of BST integration, presented as bold letters in the Table 1.4.

Table 1.4 *Requirements set by the DRAM manufacturers on the technology (or process, P) and the material system (M).*

Requirements	**Process/ Material**
Homogenous thin film deposition (< 30 nm) over large substrate areas	P
Conformal deposition of 3D structures with high aspect ratios	P
Reproducible film deposition regarding thickness and stoichiometry to ensure long term process stability	P
Compatibility to CMOS process **Low thermal budget (growth temperature below 500 °C)**	P
High throughput for high volume production	P
High permittivity (ε_r > 100) to guarantee simpler capacitor geometry for the next 1 – 2 memory generations	M
Reduced leakage current to ensure rare refresh intervals (~ 1 s) with less than 10 % charge loss due to self discharge during inter-refresh times	M/P
Development of barrier and electrode materials compatible to current CMOS processing	M
Development of novel etching processes for the dielectric material, electrodes and barriers	P
Long term degradation stability (in excess of 10 years operation stability)	M

Finally, it should be kept in mind that BST cannot necessarily be considered as the ultimate solution of the DRAM dielectric issue and soon we will face the same cell complexity problems, unless the permittivity of the dielectric is further increased. The SIA roadmap uses rather high permittivity values for BST around 700, in order to maintain the pedestal stack structure in the 0.05 μm generation and beyond, which is unachievable for the present state of the art BST films and more basic research is needed in terms of interface effects that lead to a

shrinking of the effective dielectric constant in thin films. From the above it can be concluded that the problem is focused on the charge read out, but alternative approaches are possible, like the development of resistive Random Access Memory (RAM) where the logic level is determined by resistivity measurement [23]. Ultimately, it is an economic decision, between the investment in new tools and processes for pushing the existing technology to further limits and the introduction of completely new concept.

The current trend of scaling down the dimensions of integrating circuits in order to achieve better electrical performance places serious demands for materials used in silicon based devices.

1.2 Neuroelectronic interfacing

Computer chip and brain cells and their network both work electrically [24]. However, the respective charge carriers are different, electrons in a solid ion lattice and ions in a polar fluid. Electrons in silicon have a mobility of about 10^3 cm^2/Vs, whereas the mobility of ions in water is around 10^{-3} cm^2/Vs. This enormous difference of carrier mobility is at the root for the different architecture of the two information processors. It is an intellectual and technological challenge to join these different systems directly on the level of electronic and ionic signals as sketched in Figure 1.5.

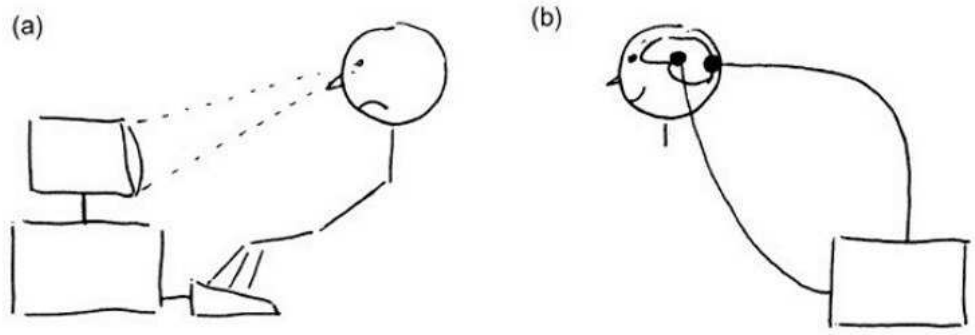


Figure 1.5 *Cartoon of brain-computer interfacing. a) Communication through the macroscopic optical and mechanical pathways screen-eye and finger-keyboard. b) Hypothetical microscopic interfacing of a computer with the visual and motor cortex [24].*

A neuron-silicon chip with an individual nerve cell from rat brain and a linear array of Si-transistors is shown in Figure 1.6. A direct coupling of ionic signals in a neuron (Appendix A.3) and electronic signals in the semiconductor can be attained by electrical polarization. An

electrical field across a membrane – as created by neuronal activity – polarizes the silicon dioxide dielectric such that the electronic band structure of silicon and the integrated transistor is affected. Vice versa, an electrical field across the silicon dioxide – as caused by a voltage applied to the chip – polarizes the membrane in a way that conformations of field-sensitive membrane proteins such as voltage-gated ion channels are affected [25-29].

Silicon is used as an electronically conductive substrate for three reasons. (i) Silicon coated with thin insulating layer is a perfect inert substrate for cultivating nerve cells. (ii) The insulating layer suppresses the transfer of electrons and electrochemical processes that lead to a corrosion of the silicon and damage of the cells. (iii) A well established semiconductor technology allows the fabrication of microscopic electronic devices that are in direct contact to the cells, covered with the inert oxide layer.

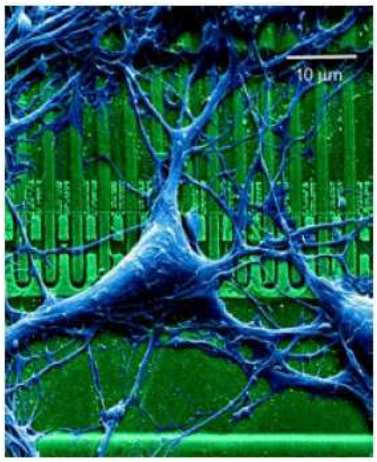


Figure 1.6 *Nerve cell from a rat brain on a silicon chip (linear array of field-effect transistor are visible as dark squares). The surface of the chip consists of thermally grown silicon dioxide (green). The neuron (blue) is cultured on the chip for several days in an electrolyte [24].*

In order to achieve the depolarization of the membrane and thus the opening of voltage-gated ion channels in the nerve cell adhered to the silicon chip, the capacitive current across the electrolyte (in electrolyte/insulator/silicon system or called EIS-system) is required (Appendix A.3). The specific capacitance of chips with silicon dioxide (SiO_2) dielectric material ($\kappa \approx 4$) was not sufficient to activate voltage-gated ion channels in the cell membrane that is the basis of neuronal excitation. To enhance capacitance, it is proposed to use the materials with high-κ dielectric constant [30]. The SiO_2 was replaced with titanium oxide (TiO_2) and hafnium oxide (HfO_2). The setup is sketched in Figure 1.7. A circular capacitors with a diameter of 250 µm was obtained by etching a thick field-oxide SiO_2 on p^{++}-doped <100> silicon ($\rho = 6 - 10$ mΩcm). A thin film of TiO_2 and HfO_2 is formed by atomic layer deposition (ALD) on a buffer layer of silicon nitride (SiN). After immersion into an electrolyte, the differential capacitance of the electrolyte-oxide-silicon (EOS) junction was measured for various bias voltages between an Ag/AgCl electrode in the electrolyte and bulk silicon.

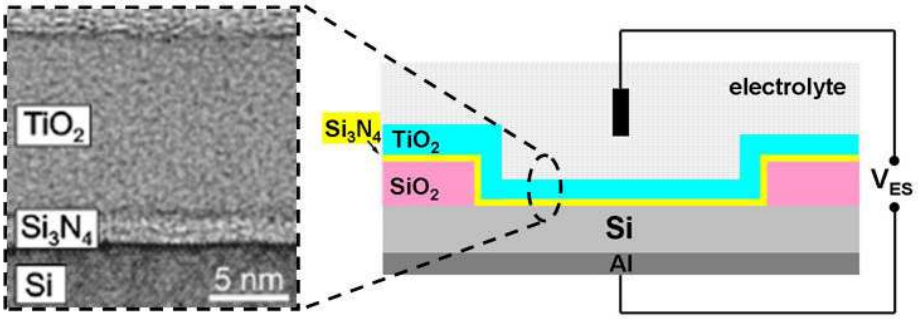


Figure 1.7 *Schematic cross section of electrolyte/oxide/silicon system [30].*

The total saturation capacitance c_{sat} of an EOS system is given by the serial capacitance densities of (i) the accumulation layer c_{acc}, (ii) an interfacial layer c_{IL}, (iii) the oxide c_{ox}, and (iv) the electrical double layer in electrolyte c_{DL}:

$$\frac{1}{c_{sat}} = \left(\frac{1}{c_{DL}} + \frac{1}{c_{IL}} + \frac{1}{c_{acc}} \right) + \frac{1}{\varepsilon_0 \varepsilon_{ox}} d_{ox} \qquad (1.3)$$

For a different thickness of TiO_2 and HfO_2 a linear relation between c_{sat}^{-1} and d_{ox} was obtained. From the slopes, dielectric constants of $\varepsilon_{ox} = 33.9 \pm 1.6$ for TiO_2 and $\varepsilon_{ox} = 15.4 \pm 0.4$ for HfO_2 were obtained, which are in good agreement with reported values [31, 32]. The system with TiO_2 and HfO_2 exhibit negligible Faraday current between −6 V and +0.5 V and between −5 V and +2 V, respectively. On that basis, EOS systems with TiO_2 and HfO_2 have been successively used for capacitive activation of K^+ and Na^+ channels in living cells [33, 34].

The concept of capacitive stimulation of ion channels is illustrated in the Figure 1.8a [35-37]. The glass micropipette filled with a concentrated salt solution served as electrode for the current recording. A human embryonic kidney (HEK293) cell was grown on a silicon chip (4 x 4 mm^2), which was insulated with 17 nm thick TiO_2 (Figure 1.8b). The capacitor fabrication is described previously. The cell membrane, with its ion channels, is separated from the chip by a thin film of the electrolyte. If the bath electrolyte is kept on ground potential ($V_E = 0$), the current conservation in the planar core-coat conductor of cell-capacitor junction is expressed by the equation [35, 36]:

$$-\frac{1}{r_J}\nabla^2 V_J = c_{ox}\left(\frac{\partial V_S}{\partial t} - \frac{\partial V_J}{\partial t}\right) + c_M\left(\frac{\partial V_M}{\partial t} - \frac{\partial V_J}{\partial t}\right) + g_K\left(V_M - V_J + V_K^0\right) \qquad (1.4)$$

where r_J is the sheet resistance of the cleft, V_J the extracellular voltage, V_S the voltage applied on the silicon substrate, V_K^0 reversal potential ($V_K^0 = -83$ mV), c_{ox} specific capacitance of

insulated oxide on the silicon, c_M specific capacitance and g_K specific potassium conductance of the attached membrane. For the homogenous area contact model and if the intracellular voltage was kept constant ($V_M = -80$ mV) with respect to the electrolyte at ground potential, the extracellular voltage V_J in the cell-silicon chip junction is determined with [35]:

$$\left(c_{OX} + c_M\right)\frac{dV_J}{dt} + g_J V_J = c_{OX}\frac{dV_S}{dt} + g_K\left(V_M - V_J - V_K^0\right) \tag{1.5}$$

Applying the voltage ramp with an amplitude $\Delta V_S = -7$ V and duration $\Delta t = 5$ ms, the stationary change of the extracellular voltage V_J for closed channels ($g_K = 0$) is [34]:

$$V_J = \frac{c_{OX}}{g_J}\frac{\Delta V_S}{\Delta t} = c_{OX}\frac{\rho_J A_J}{\eta_J d_J}\frac{\Delta V_S}{\Delta t} \tag{1.6}$$

For $c_{OX} = 1.25$ µF/cm^2, contact area $A_J = 700$ µm^2, electrolyte resistivity $\rho_J = 65$ Ωcm, distance between the cell and the chip $d_J = 50$ nm, and a geometry parameter $\eta_J = 5.78\pi$, the extracellular voltage is $V_J \approx -8$ mV. To achieve a significant activation of the K^+ voltage-gated channels, $V_J > 50$ mV is required. For that reason, NaCl as bath electrolyte was replaced by glucose with a resistivity $\rho_J = 600$ Ωcm and then $V_J \approx -80$ mV is expected.

The current across the membrane was measured with a pipette during the decaying slope $\Delta V/\Delta t$ of the voltage ramp applied to the capacitor (Figure 1.8c). If no ion pores are generated ($I_P = 0$), leakage and transient current (I_L and I_{trans}, respectively) are compensated, then the pipette current is the sum of K^+ ion current through the channels (I_K) and the capacitive current (I_{cap}) [35]:

$$I_{Pip} = I_K + I_{cap} + I_P + I_L + I_{trans} \tag{1.7}$$

$$I_{Pip} = I_K + I_{cap} = A_j\left[g_K\left(V_M - V_J - V_K^0\right) - c_M\frac{dV_J}{dt}\right] \tag{1.8}$$

Larger negative slope of the voltage ramp causes an increase of that the pipette current (up to $I_{Pip} = 10$ nA). The response was assigned to the opening of K^+ voltage-gated channels and thus to the K^+ ion current through the attached membrane, as the channels in the free membrane are closed at $V_M = -80$ mV.

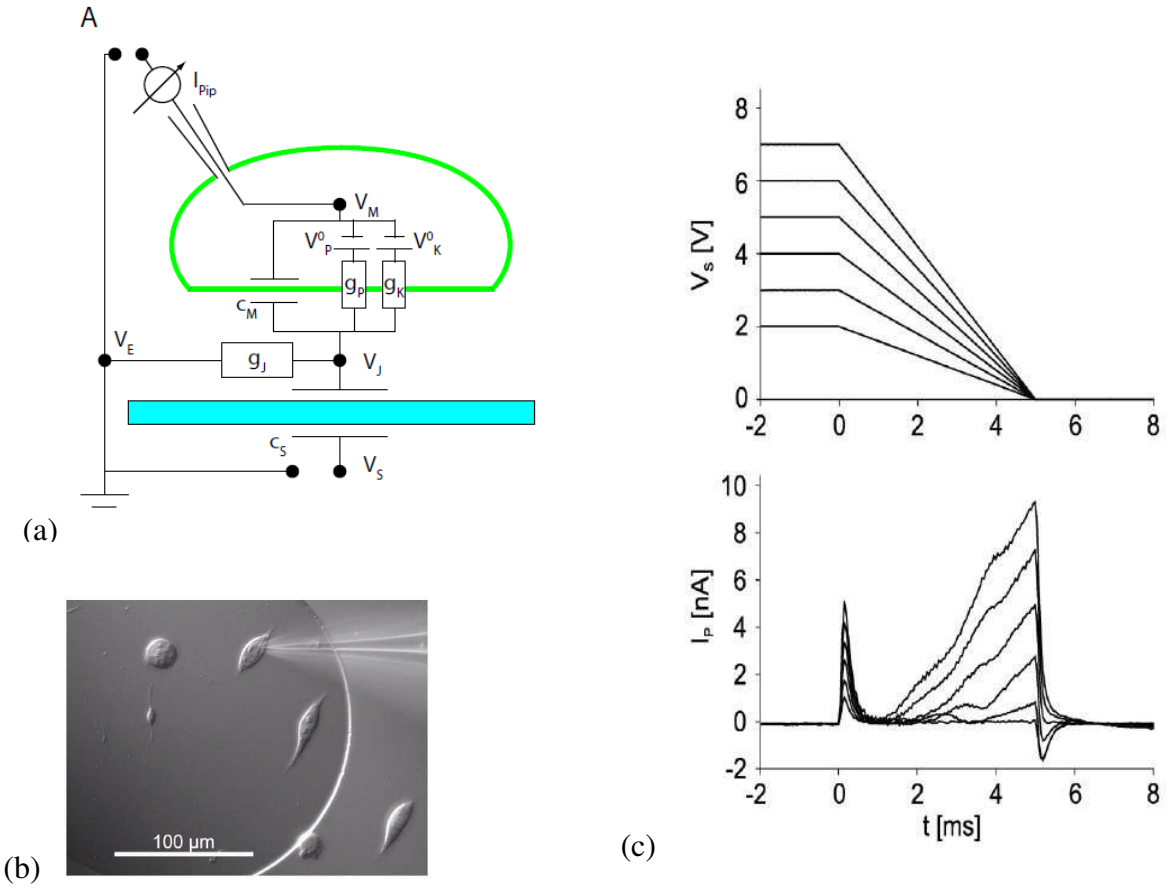


Figure 1.8 *Capacitive stimulation of Kv1.3 channels in HEK293 cell: (a) Schematic cross section of a cell on an EOS capacitor (not to scale) [35]. (b) Microscopic image of HEK293 cells on the capacitor. (c) Decaying voltage ramps V_S applied to EOS capacitor at constant intracellular voltage $V_M = -80$ mV and pipette current I_{Pip} in the attached cell membrane [37].*

1.3 Objectives of research work

The aim of this work is to develop conductive oxygen diffusion barrier which will prevent the silicon oxidation during the processing of the capacitor system: poly–Si/ barrier/ electrode/ $(Ba,Sr)TiO_3$. In that context the composition of $Ta_xSi_yN_z$ barrier will be optimised in terms of oxidation resistance, low electrical resistance and barrier properties. There are several demands for the oxygen barrier that will be introduced: It should 1) be resistant to oxidation during the high temperature processing of BST, 2) remain conductive after the deposition of high-κ material (resistivity bellow $2.6 \cdot 10^{-4}$ Ωm), and 3) free of fast diffusion paths.

Formation of any low-κ materials, such as SiO_2, will lead to a capacitance decrease since the low-κ material will be in series with the high-κ material. The barrier must also be resistant to formation of low-κ or high resistivity oxides at the electrode/barrier interface. Besides being

resistant to oxidation the barrier must also prevent the electrode material from intermixing with the Si forming low temperature silicide, which may be oxidize producing low-κ SiO_2 layers.

The present work is divided in two parts. First, the optimization of TaSiN composition and characterisation of TaSiN thin films is presented. Then, the capacitor system poly–Si/ TaSiN/ electrode/ (Ba,Sr)TiO_3 will be characterised in the second part.

Some notation need to be explained. The atomic composition of a TaSiN film is given as a percentage of elements (i.e. atomic concentration) in subscripts (e.g. $Ta_{21}Si_{57}N_{21}$). Adjacent layers are presented with a separation by slash (e.g. Si/TaSiN/BST) where the film most to the right is uppermost on the sample. Si denotes a single crystal silicon substrate.

2 Materials system

2.1 Electrodes

The high permittivity materials can be deposited by a variety of methods, which involve the processing at temperatures above 500 °C in oxygen ambient. In general, the oxide compounds cannot be deposited directly on the silicon because the interaction of the oxide materials with silicon at elevated temperatures will cause the formation of silicon oxide interface layer. As the silicon oxide has a much lower dielectric constant, the formation of the interfacial layer will reduce the effective dielectric constant. The alternative is to deposit the dielectric film on an intermediate base electrode material which has to fulfil the following requirements [38]. (i) It should remain electrically conductive after exposure to an oxidizing environment at high temperatures. (ii) It should prevent diffusion of oxygen through it to the underlying silicon substrate in order to preserve the electrical properties of the substrate. (iii) It should prevent diffusion of silicon to the electrode surface and formation the silicon oxide. (iv) It should remain smooth, uniform, and adhere well to the substrate before and after the high temperature treatment.

Noble metals are the most promising electrode materials in the processing of thin capacitors based on high permittivity materials. This is due to a combination of low resistivity and excellent stability against oxidation and reaction with the dielectric materials during elevated temperature processing [39]. However, in the direct contact geometry of noble metal with Si, it comes to undesirable formation of silicide at higher temperatures. While some silicidation may be beneficial, leading, for example, to improved electrode/Si adhesion, and/or reduced contact resistance, completely silicided noble metal electrodes are susceptible to oxidation with attendant formation of a surface layer of low-κ SiO_2 [40]. In the case of platinum (Pt) on Si, Pt and Si first react at 323 °C to form Pt_2Si, which reacts further to form PtSi [41]. In the case of iridium (Ir), the orthorhombic IrSi is the first silicide form, at temperatures as low as 400 °C [42]. Further reaction at temperatures in the 400 – 550 °C range produces semi-

conducting $IrSi_{1.75}$ (~ 1 – 5 Ωcm). Rhodium (Rh) silicide formation shares a number of similarities with Ir silicide formation. Platinum and rhodium are permeable to oxygen. Iridium forms IrO_2, which is also permeable to oxygen. The refractory metals, such as titan (Ti) and tantalum (Ta) and their binary nitrides failed as oxygen barrier layer due to their oxidation at higher temperatures [38, 43-47].

2.2 Diffusion barrier

The harmful interaction between Si and noble metal electrodes, as mentioned in the previous section, imposes the use of diffusion barriers in order to reliably fabricate a capacitor system: poly–Si/ electrode/ $(Ba,Sr)TiO_3$. The most important barrier properties are considered in this chapter. The concept of the use of barrier layers in metallization systems is simple: two materials that have unfavourable chemical interaction are kept separate by an intermediate layer. Such barrier should possess several features, which include [48, 49]:

- The barrier should prevent oxygen diffusion to poly-silicon substrate and reaction between them. Thus, the barrier should be free of fast paths for oxygen diffusion such as grain boundaries and dislocations in order to prevent the oxygen penetration to the substrate. The most preferred structure would be single crystal. A practical second choice is the amorphous structure.
- The barrier layer should form low resistance contacts with both materials, silicon and electrode material, and remain conductive after high temperature processing of high-κ materials. The resistivity of the barrier layer itself must remain bellow $2.6 \cdot 10^{-4}$ Ωm [2, 50]. Thus, the TaSiN films would have acceptable resistance (less than 1 kΩ) when patterned into plugs with 0.1 µm diameter and 30 µm thickness.
- The barrier should adhere well to all materials used in metallization scheme. Thus, some reactivity is required in order to establish good adhesion between the barrier and the surrounding materials

Practical diffusion barriers are generally divided into (a) sacrificial barriers, (b) stuffed barriers, and (c) amorphous diffusion barriers (Figure 2.1)[39]. The idea of sacrificial barrier is that the intermediate barrier material (X) reacts either with one of both materials A (poly-silicon) and/or B (electrode) in laterally uniform manner with controlled reaction rates. The effectiveness of the barrier is determined by the reaction rates. As long as the intermediate layer is not completely consumed in the reaction, the separation between the materials A and

B is still effective. Therefore, reaction rate between X and A or/and B should adequate in order to have effective barrier layer. This definite lifetime is also the major limitation of sacrificial barriers.

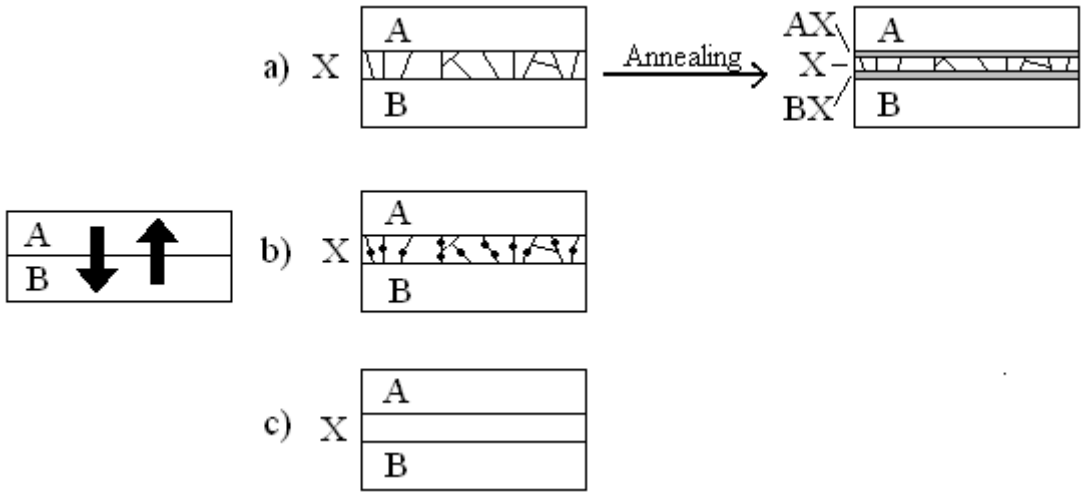


Figure 2.1 *Schematic illustration of the three classes of diffusion barrier: a) sacrificial b) stuffed and c) amorphous barrier.*

For more permanent protection the barrier layer X should be thermodynamically stable against A and B. This means that there are negligible driving forces for reactions at the interfaces A/X and X/B. This is necessary but not sufficient condition for stable diffusion barrier. It is also necessary to stop or reduce diffusion of A and B across X via fast diffusion paths, since there is still a driving force for A to diffuse into B and vice versa. This can be achieved by either (1) eliminating the fast diffusion paths or (2) fill the easy paths with appropriate atoms/molecules and thereby prevent the fast diffusion of A and B. The second approach leads to the concept of stuffed barrier. When atoms of A and B cannot use the short-circuit paths (they are now occupied by the atoms or molecules introduced there on purpose) diffusion is slowed down generally by several orders of magnitude. The elimination of short-circuit paths can also be achieved by removing the fast paths (i.e. grain boundaries) by making the structure of the barrier amorphous [5]. It is emphasized that amorphous layers are metastabile and will eventually crystallize. When crystallization takes place, grain boundaries are again present in the barrier. Thus, the crystallization temperature of amorphous layer is of critical importance.

In thin film technology there has been considerably advances in producing metastabile and amorphous films resulting from the development of the physical vapour deposition (PVD) techniques, especially magnetron sputtering. During sputter deposition, the atoms condensing in an intermixed state try to find a stabile configuration. Structural order in thin film is

produced largely by the mobility of the adatoms. Low mobility does not allow the formation of equilibrium phases and metastabile and/or amorphous phase formation is likely. Therefore phase formation and crystalline state are mainly influenced by substrate temperature together with surface and bulk diffusivities.

The amorphous films are always metastabile. For an amorphous material of given composition, there always exists a crystalline phase or mixture of several crystalline phases which are thermodynamically more stabile than the amorphous phase. In other words, amorphous phases exist only because nucleation or/and growth of equilibrium phases is prevented. Thus, there is generally a considerable large driving force for the crystallization of the film. For example, using amorphous barrier layer between silicon and copper in copper metallization scheme, the presence of copper overlayer enhances the crystallization of some underlying amorphous films. Copper, which diffuses into the amorphous layer, offers heterogeneous nucleation sites for the crystallization, thus reducing the critical nucleus size, which is required for the formation of a stable crystal [51].

Firstly, there are the several parameters that establish the effectiveness of diffusion barriers which need to be examined. And secondly, the stability of diffusion barrier during processing steps subsequent to their deposition, e.g. in oxygen ambient, has to be clarified.

The most important parameter of amorphous thin films is the crystallization temperature, which alone does not necessarily assure good thermal stability. The ternary Ta-Si-N alloy possesses the highest temperature of crystallization among the amorphous alloys [51]. Chemical inertness/reactivity of barrier material with the bordering media is the second important parameter. Therefore, it is essential to have sufficient information about possible reactions in order to predict the stability of the complete contact structure. The amorphous thin films are free of fast diffusion paths (e.g. grain boundary) and therefore, attractive for diffusion barrier properties. However, the diffusivity in barrier films has to be explored. For example, aluminium diffusion in the amorphous Ta-Si-N film is very low. However, in the gold-based metallization, the diffusion of gold in Ta-Si-N film is significant higher at temperatures above 750 °C [52]. The oxidation behaviour of diffusion barrier is relevant for the application in the metallization scheme. The stability of the diffusion barrier must be maintained during the high temperature processing of high-κ materials in oxidizing ambient.

2.2.1 Tantalum silicon nitride

The tantalum silicon nitride (Ta-Si-N) materials have been considered for use in metallization scheme as copper diffusion barrier due to their lack of fast diffusion paths and high crystallization temperatures and as gate electrode in MOSFET devices [52-61]. The same physical properties make Ta-Si-N a good choice as an oxygen diffusion barrier in stacked capacitor DRAM structures with perovskite dielectrics [62-76]. In Figure 2.2 the location of the barrier layer (Ta-Si-N) in a generic stacked-capacitor structure is schematically depicted. The barrier is used to separate the lower electrode (Pt) from the plug (doped polycrystalline Si). A high dielectric constant material (e.g. BST) is sandwiched between the upper and lower electrodes (Pt) while the poly-Si plug makes contact to the junction region of the complementary metal-oxide semiconductor (CMOS) device. A low-κ material such as SiO_2 is used to insulate doped plug regions. High dielectric constant materials, such as BST, typically require deposition at high temperature (550 – 700 °C) in the presence of oxygen and/or post-deposition anneals at high temperature in oxygen in order to form the desired high-κ perovskite phase [77].

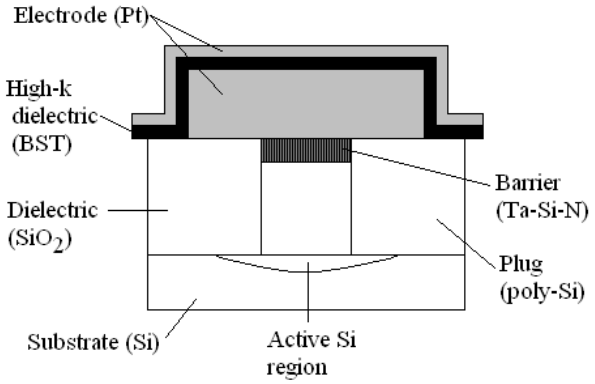


Figure 2.2 *A schematic representation of an elementary stacked-capacitor electrode-barrier structure showing the placement of the barrier layer (Ta-Si-N) between the lower electrode (Pt) and plug (polycrystalline Si).*

This makes the requirements for a barrier material like Ta-Si-N in a stack capacitor structure quite demanding. The barrier must be resistant to oxidation and remain adequately conductive, and prevent oxygen diffusion to the poly-silicon plug interface which could lead to SiO_2 formation. Formation of low-κ materials, such as SiO_2, will lead to a capacitance decrease since the low-κ material will be in series with the high-κ material:

$$\frac{1}{C_e} = \sum_{i=1}^{n} \frac{1}{C_i} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{BST}} \qquad (2.1)$$

The barrier must also be resistant to formation low-κ material or high resistivity oxides at the electrode-barrier (TaSiN/Pt) interface. Besides being resistant to oxidation the barrier must also prevent the electrode material (Pt) from intermixing with plug poly-Si. Otherwise, Pt and Si will form low temperature silicides (< 300 °C) which will oxidize, producing low-κ SiO_2 layers.

The diagram in the Figure 2.3 shows the Ta-Si-N composition range, identified as optimum, for use as oxygen diffusion barriers in stacked-capacitor DRAM structures proposed by Cabral *et al.* [10]. The optimum Ta-Si-N compositions are in the range Ta (20 – 25 %) – Si (20 – 45 %) – N (35 – 60 %). After annealing at 650 °C for 30 min in pure oxygen TaSiN thin films with optimum compositions showed resistivities below $2.6 \cdot 10^{-3}$ Ωm, surface area oxygen densities less then $1 \cdot 10^{17}$ atm/cm^2, no interdiffusion of platinum (Pt) and silicon (Si), no detectable SiO_2 formation at the barrier-Si plug interface and amorphous/nanocrystalline microstructure. For optimum oxygen diffusion barrier there is a compromise between high concentration of Ta for low resistivity, high concentrations of Si for oxidation resistance and high concentration of N for high temperature crystallization.

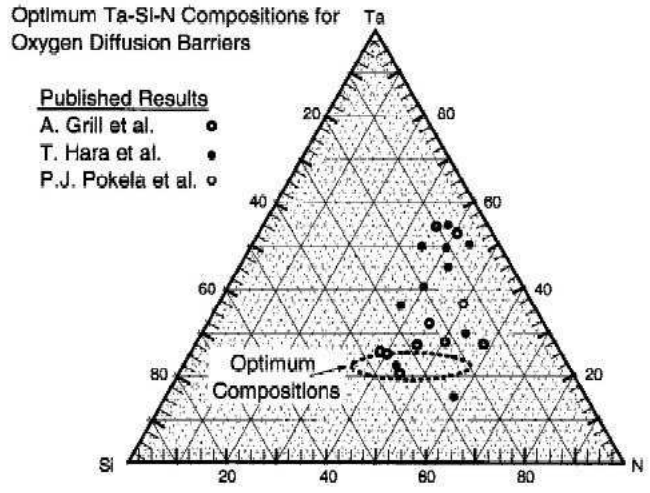


Figure 2.3 *Ternary phase diagram showing the range of optimum Ta-Si-N compositions for use as oxygen diffusion barrier as compared to those reported by other authors [10].*

2.3 Properties of high-permittivity dielectrics

There are numerous materials with higher permittivity than ONO ($SiO_2/Si_3N_4/SiO_2$) films, but only a few of them are serious candidates for use in an ultra-large scale integrated DRAM cell as the capacitor dielectric. The most relevant requirements are listed for a thin film dielectric

with high permittivity to be integrated into a capacitor of a DRAM 1T−1C cell in a CMOS chip of an advanced Gb generation [77]:

- High permittivity ($\varepsilon_r > 200$) to guarantee simpler electrode geometries, i.e. lower 3D trench factor, for several DRAM chip generations. A charge of about 25 fC at voltages ≤ 1 V has to be loaded to the cell capacitor. This corresponds to a usable cell capacitance $Cs \geq 25$ fF.
- The material has to be homogenously deposited as a thin film with thickness of ≤ 30 nm over large areas (12" wafer size). The deposition method has to ensure a conformal coverage in order to coat 3D structures. The thermal budget should be as low as possible. For these reasons, the metal-organic chemical vapour deposition (MOCVD) technique is most suited for the deposition.
- As the read and write times will approach 1ns, the dielectric behaviour should not show significant dispersion up to frequencies of a several GHz.
- Refresh times of the order of 1s are desirable. Within the refresh time, the charge loss due to polarisation relaxation and leakage currents has to be smaller than 10 %.
- Long term stability of the properties (10 years is the projected life time) is indispensable.
- All the processes for the dielectric material itself as well as for the electrodes and the possibly necessary diffusion barrier and adhesion layers have to be compatible with the CMOS process technology.

The most promising candidate material is barium strontium titanate, $(Ba,Sr)TiO_3$ (BST). The bulk ceramic of BST reaches the permittivity values up to 10 000. There are several other mixed oxides with permittivities of several thousands to ten thousands in bulk ceramics, e.g. in the lead/titanium system such as $(Pb,La)(Zr,Ti)O_3$ (PLZT) and $Pb(Mg,Nb)O_3$-$PbTiO_3$ (PMN-PT) [78]. Such materials are ferroelectric in general, but for special stoichiometries they are paraelectric, or their hysteresis loop is very narrow, i.e. the coercive field is sufficiently small that can be used as dielectric in a DRAM capacitor. It has to be proven whether these materials can retain the high permittivity as the thickness is reduced into 10 nm range.

2.3.1 Barium strontium titanate

Barium strontium titanate $(Ba,Sr)TiO_3$ (BST) has the perovskite crystal structure of the general type $A^{2+}B^{4+}O^{2-}{}_3$, as shown in Figure 2.4a and can be considered as a solid solution of strontium titanate, $SrTiO_3$ (STO), and barium titanate, $BaTiO_3$ (BTO) [79]. The name perovskite comes from the mineral ($CaTiO_3$), but is now used to describe a whole class of materials with the same cubic structure or similar, but distorted crystals. The large A^{2+} cation in the perovskite lattice is coordinated with twelve oxygen ions and represented by Sr^{2+} or Ba^{2+} cations with similar ion radii. The smaller Ti^{4+} cation in the B position is in the middle of an octahedron of O^{2-} anions and is coordinated with six oxygen ions.

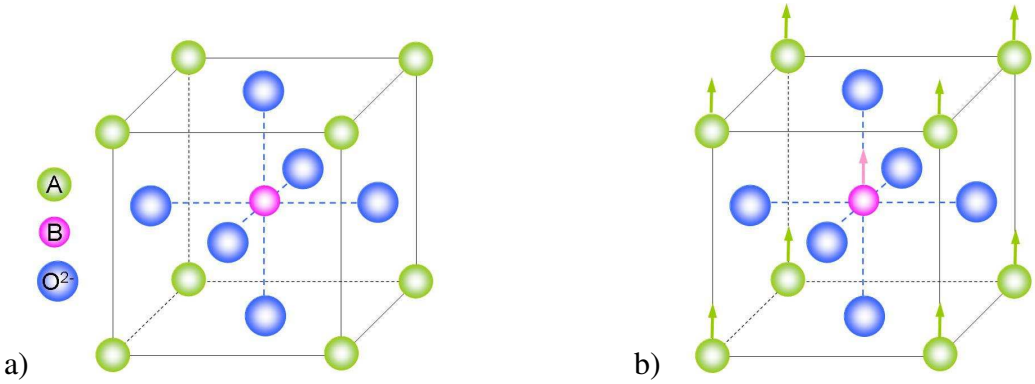


Figure 2.4 *a) Cubic perovskite cell b) The arrow indicates the displacement of the Ti^{4+} ion at the transition to the tetragonal structure.*

The distortion of the cell structure strongly depends on the ionic radii of the cations and the different phases. The different phases of bulk ceramics have been summarized in Figure 2.5. The figure shows that $SrTiO_3$ has a cubic cell structure at a room temperature and consequently must be paraelectric. However, $SrTiO_3$ shows a structural phase transition from cubic to a tetragonal phase at 105 K and from tetragonal to an orthorhombic phase at 65 K [80]. At temperatures above 105 K STO has the cubic cell structure. Cubic $BaTiO_3$ displays phase transformation at 396 K and is tetragonal at room temperature [81]. This tetragonal structure is expressed in the displacement of the Ti^{4+} ions in the crystal lattice (Figure 2.4b) and is ferroelectric at room temperature. These two materials can be fully intermixed into $(Ba,Sr)TiO_3$ (BST), so that the phase transition (cubic to tetragonal) is adjustable over a wide temperature range. For bulk $(Ba_{0.7},Sr_{0.3})TiO_3$ ceramic the phase transition temperature is 310 K [82].

The paraelectric to ferroelectric transition occurs simultaneously with the phase transition from cubic to tetragonal. The transition is also associated with a strong rise of the

permittivity, which reaches values up to 5000 for $BaTiO_3$ bulk ceramic [82]. In the cubic phase the permittivity $\varepsilon_r(T)$ and susceptibility dependence on temperature obeys the empirical Curie-Weis law:

$$\varepsilon_r(T) \approx \varepsilon_r(T) - 1 = \chi(T) = \frac{C}{T - T_C} \qquad \text{for } T_C < T_0 < T \qquad (2.2)$$

where C is the Curie-constant and T_C is the Curie-temperature which in general is smaller than the temperature T_0 of the phase transition the cubic to tetragonal structure. The constants for $SrTiO_3$ bulk ceramic are $C = 7.83 \cdot 10^4$ K and $T_C = 28$ K and for $BaTiO_3$ are $C = 1.5 \cdot 10^5$ K and $T_C = 388$ K [83, 84].

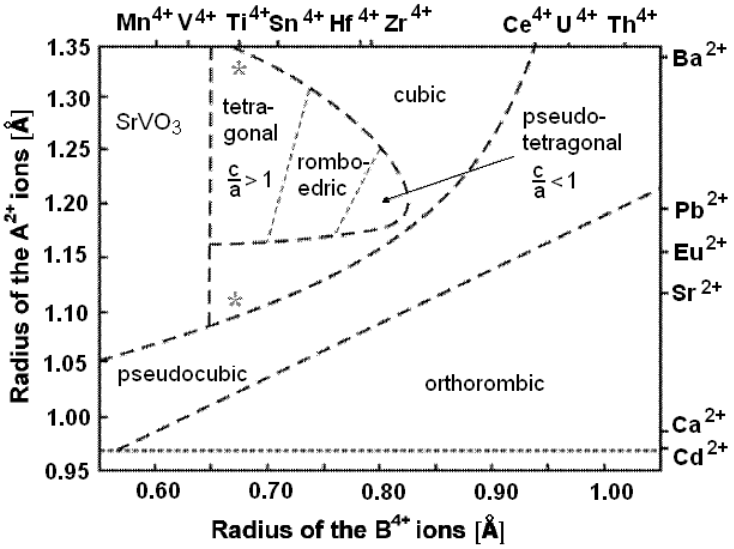
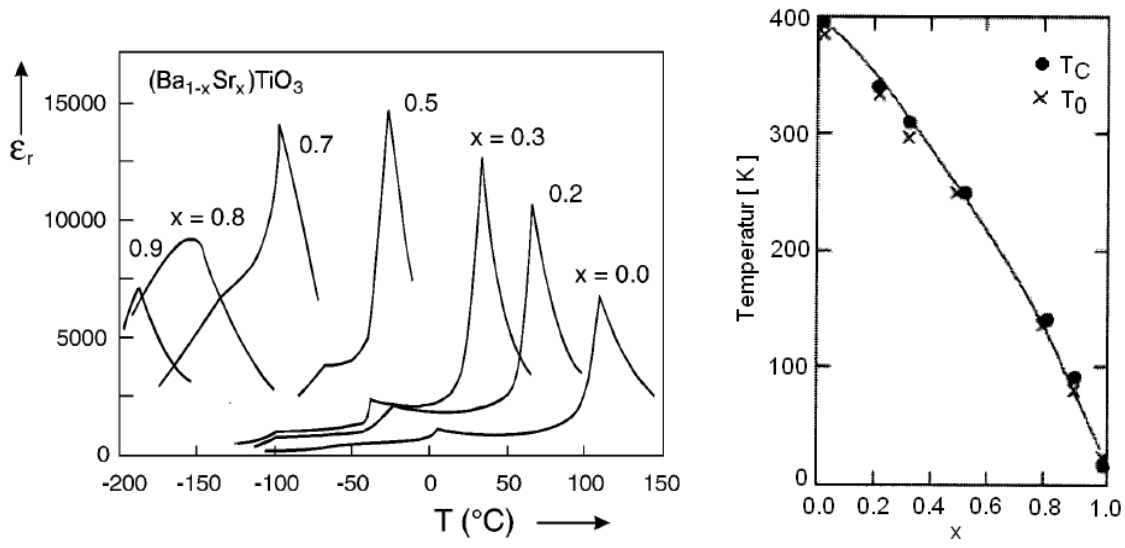


Figure 2.5 *Distorted perovskites ABO_3 and their dependence on the ion radii R_A and R_B at room temperature [83].*

As illustrated in Figure 2.6, which shows the temperature dependence of the low frequency dielectric constant in $(Ba_{1-x},Sr_x)TiO_3$ ceramics in the compositions from $x = 0$ ($BaTiO_3$) to $x = 1$ ($SrTiO_3$), the ferroelectric transition of BST can be shifted in the temperature by adjusting the Ba to Sr ratio in the BST lattice. For bulk ceramics this maximum is near room temperature for Ba:Sr ratio 7:3 ($T_C = 297$ K and $T_0 = 310$ K) [82].



a) b)

Figure 2.6 *BST ceramics with different compositions ranging from BTO to STO: a) temperature dependence of the permittivity b) Composition dependence of the transition (T_0) and Curie (T_C) temperature.*

Thin films with thickness < 1µm display a deviation from these properties. This different behaviour may be induced by grain size effect, as well as the substrate properties like thermally induced stress due to different thermal expansion coefficient or interfacial space charges. Thin BST films display a strong deviation of the permittivity compared to the bulk case as can be seen in Figure 2.7 [85]. The permittivity values lay in the region $\varepsilon_r \sim 250 - 1000$. The maximum of the permittivity for thin films is spread over a rather wide temperature range, which is advantageous for device operation. On the other side, the permittivity of thin films is lower by at least 1.5 order of magnitude compared to bulk, but still remains high compared to conventional ONO dielectrics. The drop in the permittivity may be interpreted by the effect of a low permittivity interfacial layer of 0.5 to 2 nm thickness at the grain boundaries ("dead layer") [77]. This layer shows no difference of the composition and crystal structure in comparison to the bulk and is believed to be photonic structure [86].

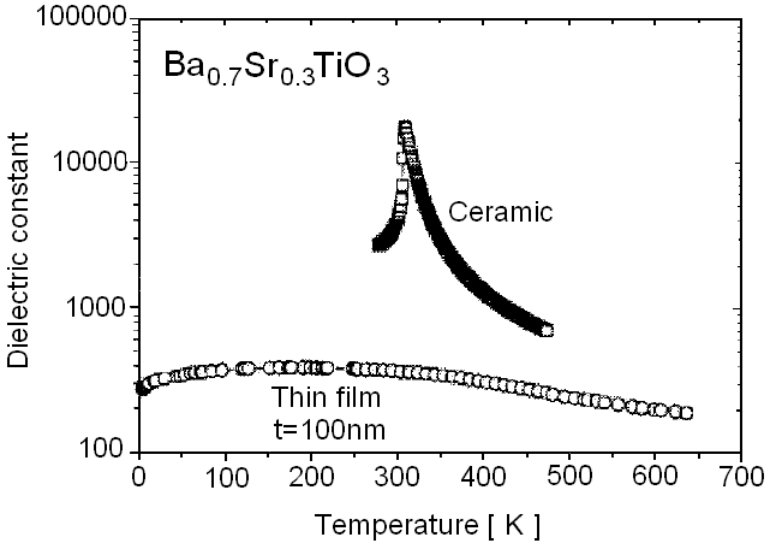


Figure 2.7 *Temperature dependence of the permittivity for ceramic and 100 nm ($Ba_{0.7}Sr_{0.3}$)TiO_3 thin film (MOCVD grown films) [85].*

Current DRAMs have read pulses below 10ns which corresponds to 100 MHz and these times will continue to decrease. The frequency dissipation of permittivity and dissipation factor was studied between 10 kHz and 20 GHz [87]. A constant dispersion of the capacitance in the range of 5 % was observed over the measurable frequency range (Figure 2.8). The dissipation loss (*tan δ*) appeared to increase above 1 GHz by factor two (but could be due to non-ideal measuring conditions).

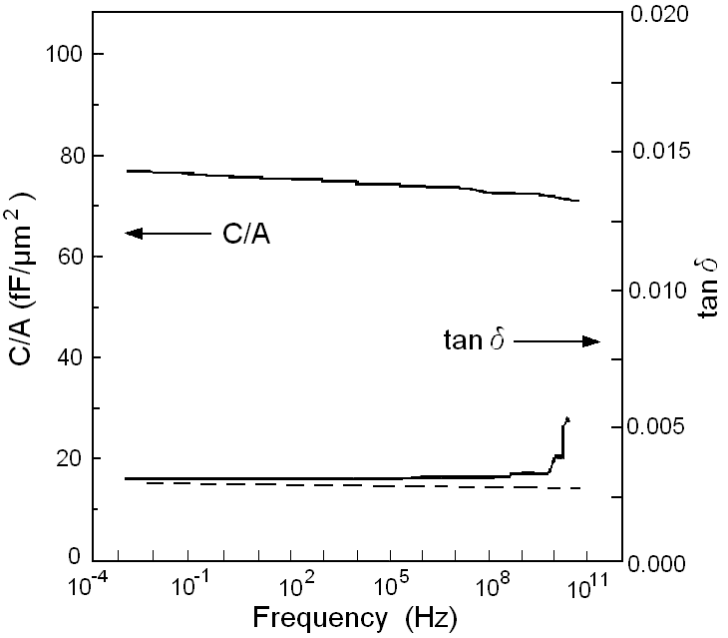


Figure 2.8 *Frequency dissipation of capacitance area density and tan δ for BST thin film [87].*

Like many of the high-κ materials BST is a non-linear dielectric, i.e. the induced polarization displays a non-linear dependence on the applied field. This effect becomes also thickness dependent for thin films and is demonstrated in Figure 2.9a [87]. The capacitance increases with decreasing thickness as expected. For voltages $|U| < 1$ V, which are interesting for application, the C/A values are above 30 fF/μm^2, which is equivalent with permittivity of approx. 250 at zero bias, and sink dramatically (< 100) at voltages larger than 5 V. This characteristic can be used in tunable devices and filters. The calculated permittivity (Figure 2.9b) indicates the quantitative behaviour more clearly and displays a decreasing maximum capacitance with decreasing thickness. This behaviour is an indication that the "dead layer" have to be considered in the quantitative description.

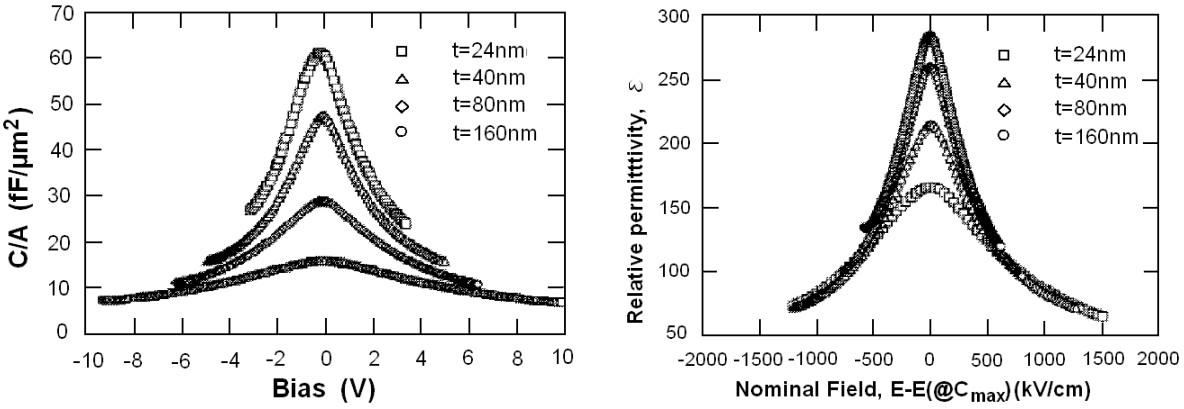


Figure 2.9 *a) Capacitance area density vs. bias voltage for the BST samples with different thickness b) Permittivity vs. electrical field for BST thin films with different thickness (MOCVD grown films)[88].*

3 Thin film deposition

The variety of thin film deposition techniques were developed in last few decades. The right choice of deposition methods is determined by thin film application and influenced by the film and substrate properties. Nevertheless, the deposition parameters have the great influence on the structural and electrical properties of deposited material.

Thin film growth is based on physical and chemical methods. Deposition is followed from vapour or liquid phase. The deposition techniques are summarised in the Table 3.1.

Table 3.1 *Physical and chemical deposition methods.*

Physical methods	Physical vapour deposition (PVD)	Liquid phase deposition (LPD)
	• Sputter deposition • Pulsed laser deposition (PLD) • Electron beam evaporation • Molecular beam epitaxy (MBE)	• Liquid phase epitaxy
Chemical methods	Chemical vapour deposition (CVD)	Chemical solution deposition (CSD)
	• Metal organic chemical vapour deposition (MOCVD) • Plasma enhanced MOCVD (PE-MOCVD) • Metal-organic molecular beam epitaxy (MOMBE)	• Sol/Gel process • Metal organic decomposition (MOD) • Electrochemical deposition

The deposition techniques used in this work will be described in the following chapter. The TaSiN barrier, platinum and iridium electrodes were fabricated by sputtering. The patterned

platinum electrode was produced by electron beam evaporation. The dielectric thin films were deposited using sol-gel process and pulsed laser deposition.

3.1 Sputtering

The sputtering process in its many forms is perhaps one of the most utilized physical vapour deposition techniques [89-91]. Sputter deposition involves the deposition of particles that originate from a target surface being sputtered. The process is realized in a closed recipient, which is evacuated to a high vacuum before the deposition starts.

The working gas is a noble gas, usually argon. The gas is fed into the chamber up to the pressure between 0.5 to 12 Pa. The plasma is ignited by applying a negative potential of several hundreds volts to the conductive target (DC sputtering: Figure 3.1). The Ar^+ ions are accelerated toward the target, resulting in collision with and ejection of target atoms and production of secondary electrons. These electrons cause the further ionisation of working gas.

To increase the ionisation by emitting secondary electrons and subsequently to increase the deposition rate the magnet on the back side of target is used (magnetron sputtering). The magnetic field is used to trap the electrons close to the target and force them to spiral path, increasing a probability of electron-atom collision and thus ionization probability ($Ar + e^- \rightarrow Ar^+ + 2e^-$). The highest sputtered yield happens in the region where the magnet is mounted and is recognised by extensive target erosion.

The bombardment of a non-conducting target with positive ions would lead to a charging of the surface and a shielding of the electric field. The ion current would tend to zero. But using the rf-sputtering (radio frequency) by applying an ac-voltage to the target allows in one phase (negative potential to the target) that the ions are accelerated toward the target surface (Figure 3.2).

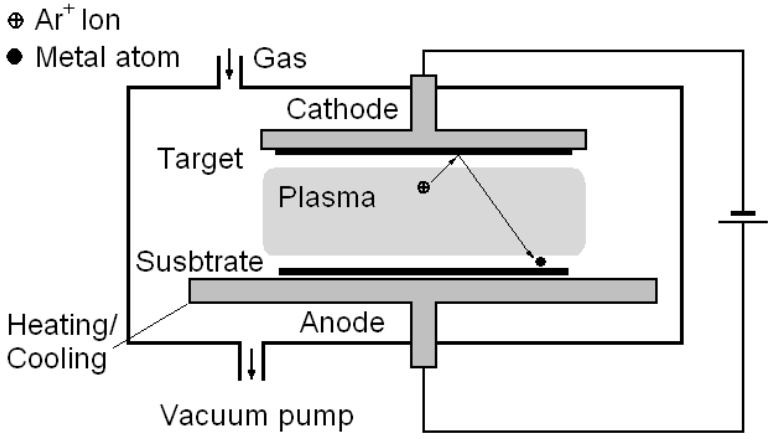


Figure 3.1 *The principle of dc-sputtering process.*

At high frequencies the massive ions only respond to the average electric field, while the electrons move to and away from the electrodes. The insulator target surface alternates between low negative potential and high negative potential in respect to plasma. The Ar^+ ions are extracted from rf plasma during the highly negative cycle and may be used to sputter the insulator surface.

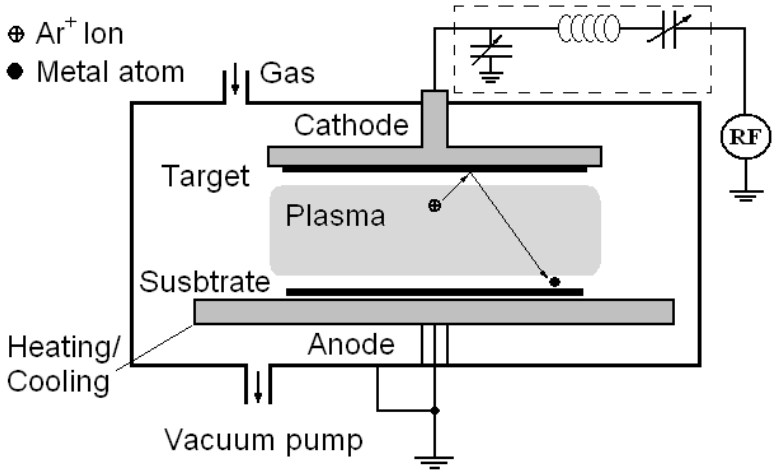


Figure 3.2 *The principle of rf-sputtering process.*

The radio frequency range spreads from 3 kHz to 30 GHz. Typically the rf systems operate at 13.56 MHz. Even though electrons and ions have different masses, at the frequencies lower then 500 kHz, both the electrons and ions can follow the variations in electric filed. Above about 3 MHz the inertia of the ions prevent them from rapidly responding to the electric field, whereas the electrons will still follow the electric field.

Introducing a reactive gas (e.g. oxygen, nitrogen or acetylene) in the chamber enables the formation of compounds. By reactive sputtering different compounds such as oxides, nitrides or carbides can be deposited.

Table 3.2 *Sputter yields for some elements as a function of Ar^+ kinetic energy [91].*

Element	300 eV	500 eV	1000 eV
Ta	0.3	0.5	0.9
Ti	0.3	0.5	0.7
Si	0.3	0.7	1.0
Pt	0.7	1.0	1.6
Rh	0.7	1.0	1.7

The sputter yield is the ratio of the atoms ejected from a target to the number of incident particles. It determines the deposition rate and depends on the chemical bonding of the target atoms, chamber pressure, the kinetic energy, the mass and the incidence direction of bombarding ions. The sputter yields for elements used in this work are given for argon ion bombardment at several energies and argon pressure 0.5 Pa (Table 3.2). Typically it is in the range 0.1 to 3. The numbers should be taken as approximate, because over the years yields have been often measured in flawed experiments [92, 93].

The resulting film properties are influenced by different parameters. The sputter current I_{sp} determinates the deposition rate and hence the growth process. The applied voltage determines the energy of sputtered particles and sputter yield. The pressure p in the chamber determines the mean free path λ for the sputtered material ($\lambda \sim 1/p$) and how many collisions occur for the particles on their way to the substrate. This can influence the film porosity, crystallinity and the texture. Varying the gas mixture one can control the film stoichiometry. The reactive gas flow can be varied, while the total pressure is kept constant by regulation of the argon flow. The substrate temperature has the strong impact on the growth behaviour and hence on film crystallinity and density.

3.2 Pulsed laser deposition

Pulsed laser deposition (PLD) is very attractive method for preparation of thin films [94, 95]. The main advantage of PLD over the other conventional deposition techniques is the possibility to deposit multi-component ceramic compounds with the same composition as the target. The wide variety of target material can be applied: metals, ceramic, polymers. The

process can take place in vacuum or in oxygen atmosphere (oxygen pressure is in the range 0.3 – 1 mbar for oxide films) or in reducing atmosphere (Ar/H_2 for superconducting MgB_2) or in inert gas (such as Ar). The typical set-up is shown in Figure 3.3.

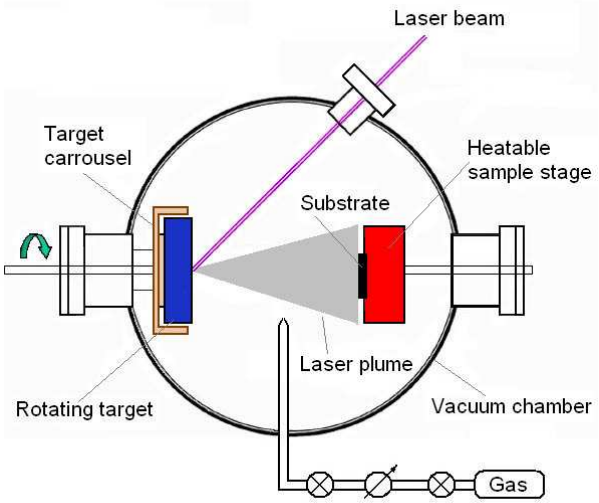
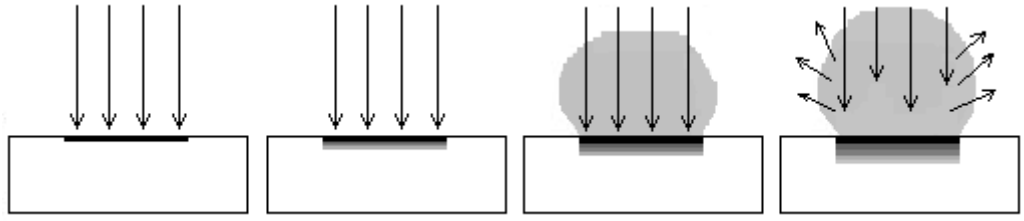


Figure 3.3 *Simplified set-up of PLD system for the thin film deposition.*

One of the most frequently used excimer laser is the KrF which operate at 248 nm [95]. For the thin film deposition the wave length in the range 200 – 400 nm is used due to strong absorption of target material in this spectral region. Absorption coefficient increases when moved to shorter wave length and the penetration depth decreases. The excimer lasers are available with different incident energy (max 1 J), pulse duration (10 – 25 ns) and maximal repetition rate 50 Hz.



a) b) c) d)

Figure 3.4 *Schematic illustration of ablation process in the case of PLD process ($L_o < L_t$): a) absorption of laser radiation b) melting of target surface c) target vaporization d) plume propagation.*

The interaction mechanism of laser pulse with matter depends on the pulse duration. In the case of picosecond and nanosecond laser pulse, the laser beam strikes the target surface and one fraction of energy will be absorbed. The absorption length depends on the absorption coefficient:

$$L_o = \frac{1}{\alpha} \tag{3.1}$$

where α is the absorption coefficient. If the absorption length is greater then the thermal diffusion length L_t given by the equation (3.2) the surface will be heated to the L_o.

$$L_t = \sqrt{\frac{2\delta_t \kappa}{c\, n_{mol}}} \tag{3.2}$$

Where δ_t is the pulse duration, κ the thermal conductivity, c the molar heat capacity and n_{mol} is the molar density of the target. This is the situation of ceramic materials. For the metals the situation is opposite. The absorption length is much smaller then thermal diffusion length (Figure 3.4). The surface starts to melt and to vaporize after approx. 100 ps. The energy above the threshold laser fluence has to be reached in order to have vapour phase of the target material. For ceramics the threshold value is around 1 J/cm^2, for noble and transition metals the values are in the range 1 – 2 J/cm^2 but for the refractory materials are higher then 10 J/cm^2.

The particle cloud which consists of evaporated material absorbs the significant part of the incoming laser beam being partially ionized. The plasma expands away from the target and the spreading of the plasma plume is modelling by $sin^n\theta$ law, where n is in the range 1 to 10 and depends on the material and the ablation parameter and θ is the scattering angle. And finally, the ablated species condense on the substrate, with the position opposite to the target, forming a thin layer.

The advantage of PLD over the other physical vapour deposition methods is that the stoichiometry of the target could very well reproduce in the thin film. Especially for the oxygen containing targets/films is observed the oxygen deficiency in the film. The disadvantage is the small area that could be coated only ~ 1 cm^2 and poor coverage of edges and sidewalls of structures.

In this work was used KF excimer laser to fabricate the BST thin films. The parameters used for the deposition of the BST films can be summarized as follows:

- oxygen partial pressure: $p(O_2)$ = 0.25 mbar,
- oxygen flow rate: 140 mln/min,
- laser energy: E = 100 mJ,
- deposition rate: ~ 50 nm/min.

3.3 Electron beam evaporation

Electron beam evaporation is a physical vapour deposition process which takes place in a high vacuum (< 10^{-5} Pa) or in ultra high vacuum (< 10^{-7} Pa) with desired purity [90]. The atoms or molecules from the vaporized source reach the substrate (line of sight deposition) without collision with residual gas in the vacuum chamber and condense onto the oppositely placed substrate. In the Figure 3.5 the vapour pressure for some materials is presented as a function of temperature. The material is heated to the temperature where the vapour pressure is above a certain limit, e.g. 1 Pa in order to have a high vaporization rate and a reasonable deposition rate.

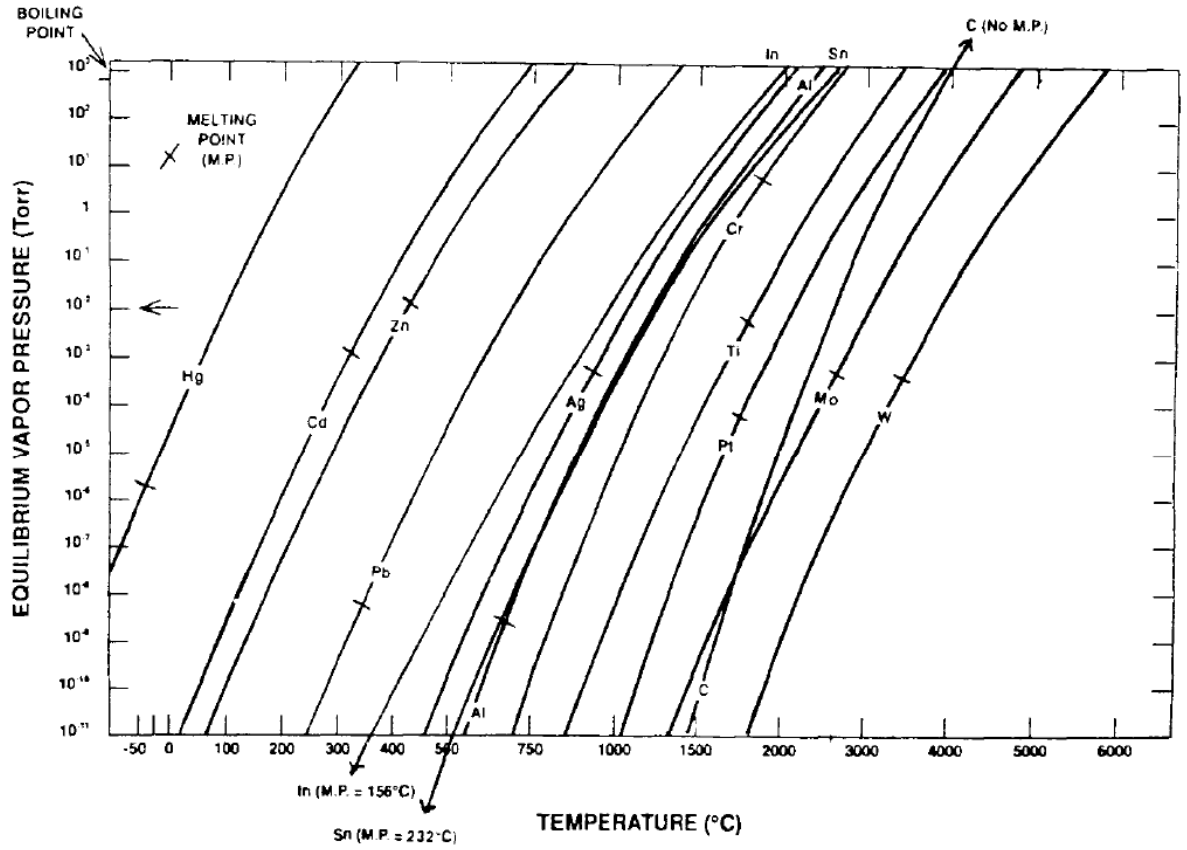


Figure 3.5 *Equilibrium vapour pressure for some materials [90].*

The commonly used heating techniques include resistive heating, high energy electron beams, low energy electron beams and inductive (rf) heating. The resistive heating is usually used for the material that vaporized at temperature below 1500 °C and the focused electron beam for the materials above 1500 °C. The high energy electron beam is formed using thermionic emission from a filament to generate free electrons, which are then accelerated using high voltages (10 – 20 kV). The beam is focused by electric and/or magnetic field onto the material surface to be evaporated (Figure 3.6). Usually the electron beam is deflected more

then 180° magnetically in order to prevent the deposition of evaporated material on the filament. The material to be evaporated is usually placed in water cooled copper crucible. Sometimes insets made from different materials, so-called liners, are necessary. It is also possible to have more then one crucible containing different materials, so that the several materials can be evaporated moving the electron beam or the crucibles, producing multilayer films.

Main advantages of this technique are that the high purity thin films can be obtained easily using high purity source materials, high deposition rate and that it is relatively inexpensive, compared to other PVD techniques. The contamination with residual gases is minimized using high or ultra high vacuum.

In this work a platinum top electrode was deposited using electron beam evaporation in ultra high vacuum (10^{-8} Pa). The accelerating voltage was 10 kV and the electron source was wolfram filament.

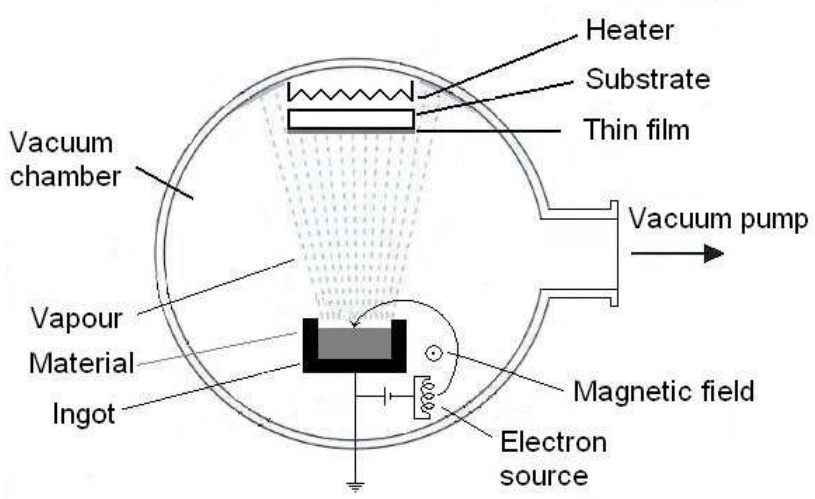


Figure 3.6 *Electron beam evaporation set-up.*

3.4 Chemical solution deposition

The development of chemical solution deposition (CSD) processes for the fabrication of the thin films with perovskite structure dates to the mid-1980s [96-99]. The method is very attractive due to the possibility to produce the variety of compositions with the perovskite structure (ABO_3) with relatively simple and low cost apparatus.

The fabrication of thin films by CSD involves four basic steps: (1) synthesis of the precursor solution with the desired cations, (2) deposition of the solution by spin-coating or dip-coating, (3) low temperature heat treatment for the removal of the organics (drying and pyrolysis) and formation of an amorphous film, (4) and high temperature heat treatment (usually under oxygen atmosphere) for densification of the amorphous layer and its crystallization. The final three steps are similar for most solution deposition approaches, despite differences in the characteristics of the precursor solution.

The precursor solution of perovskite materials synthesis involves the use of metallo-organic compounds that are dissolved in common solvent. The starting reagents are metal alkoxide compounds, $M(OR)_x$, metal carboxylates, $M(OOCR)_x$, and metal β-diketonates, $MO_x(CH_3\text{-}COCHCOCH_3)_x$. The selection of the starting compounds is dictated by a variety of factors like solubility and reactivity of reactant, decomposition pathway and stability. The solution route usually determines the degree of intermixing the cations species, the carbon content in the films and the temperature at which the pyrolysis of the organic species starts the densification and crystallisation behaviour of the films.

The CSD approaches may be grouped in three categories which are mainly different in the precursor solution: (1) sol-gel process that uses 2-methoxyethanol as a reactant and solvent, (2) hybrid or chelate process that uses modifying ligands such as acetic acid or acetylacetone and (3) metalloorganic decomposition (MOD) route that uses large metal carboxylate compounds.

In this work the hybrid process was used for fabricating $BaTiO_3$ (BTO) and $(Ba_{0.7}Sr_{0.3})TiO_3$ (BST) thin films. The scheme for film deposition is presented in the Figure 3.7.

(1) Precursor solution

It is characteristic for the hybrid process that the A-site precursors are carboxylate based and B-site precursors are alkoxides. The A-site carboxylate precursor is usually dissolved in corresponding carboxylic acid because their limited solubility in alcohols. Acetylaceton (2-4 pentanedione) is often used as a chelating agent for the B-site alkoxide. The B-site alkoxide precursors react with carboxylic acid (acetic or propionic acid) and form oligomers:

$$n\ Ti(OR)_4 + 2n\ R'COOH \rightarrow RO[\text{-}Ti\text{-}O\text{-}](OOCR')_2R + ROH$$

The chelation of the B-site cation leads to precursors which are less sensitive towards hydrolysis. In comparison to sol-gel processes with 2-methoxyethanol solvent, the hybrid processes are easier to synthesize. For synthesis of typical BTO solution the barium acetate or

propionate is dissolved in the corresponding acid. The titanium alkoxide is stabilized with acetylacetone and then these two solutions are mixed together.

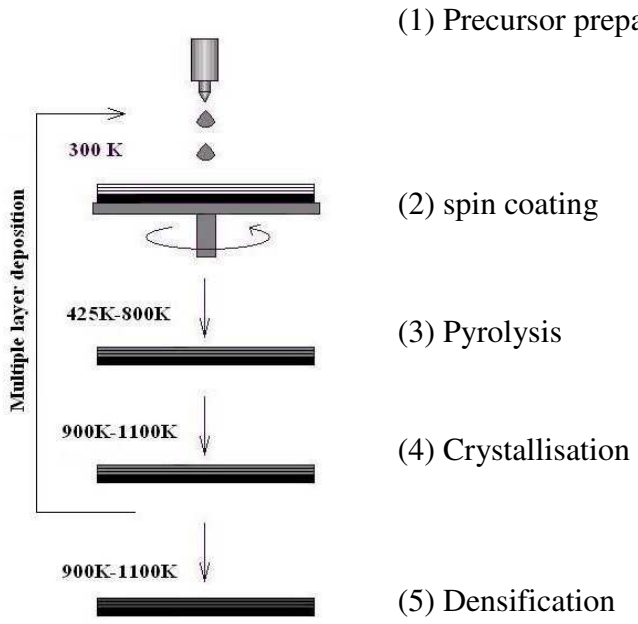


Figure 3.7 *The scheme for CSD film deposition.*

(2) Spin coating

The precursor solution is applied on the substrate surface (bottom electrode) using spin coating. After filtering through Teflon filters the precursor solution is dispersed homogenously for few seconds at the lower speed (500 rpm) and then set to the maximal speed (4000 rpm) in order to achieve thinner wet film.

(3) Pyrolysis

During the initial drying step at lower temperatures (425 K – 525 K) most of organic solvent is removed from the film. This step is followed by pyrolysis and the decomposition of precursor (600 K – 800 K). During this phase the films may shrink by 50 – 70 %.

(4) Crystallisation and (5) densification

The crystallisation and densification take place at higher temperatures, usually between 900 K and 1100 K. The solution concentration and the thickness of amorphous layer are optimized to force the nucleation at the interface of the bottom electrode and the amorphous layer. Therefore the crystallized films in the diffusion furnace have a columnar structure. When using a solution concentration of 0.1 M it leads to film thickness of around 8 nm per layer and for 0.3 M solution it is usually 27 nm (for spin speed of 4000 rpm).

The substrate, solution chemistry, and thermal processing conditions can have significant effect on the thin film microstructure and orientation [100]. Thus, microstructural differences and orientation lead to differences in electrical and optical properties of thin film.

4 Thin film analysis: structural and electrical properties

In this chapter a description of the experimental procedures and methods for the characterization of thin films is given. Methods for structure analysis and electrical characterization of thin films along with the details of the instruments used will be described.

4.1 Structure and morphology

4.1.1 X-ray diffraction

The fabricated samples have been analyzed by X-ray diffraction (XRD), concerning their crystallographic orientation and texture. The XRD measurements were preformed using a Philips X'PERT diffractometer with a CuK_α cathode (characteristic wavelength $\lambda = 1.5418$ Å). The diffractometer was used in the Bragg-Brentano ($\theta-2\theta$) (Figure 4.1) and the glancing angle incident (GIXRD) geometry. For GIXRD mode the incident beam was fixed at 1°. In this mode the penetration depth is smaller and therefore more sensitive to the any phase present in thin film without substrate interference. For example, for CuK_α radiation the penetration depth of silicon is 67.7 µm but using GIXRD geometry and for glancing angle $\alpha = 1°$, the penetration depth is 1.06 µm [101].

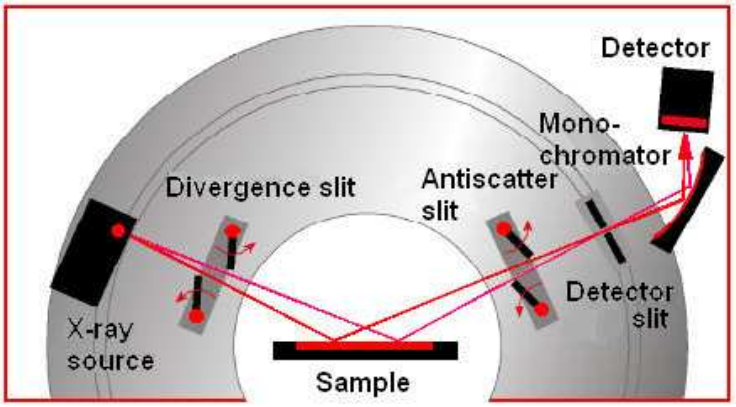


Figure 4.1 *Bragg-Brentano geometry (θ-2θ geometry).*

For a periodic crystal structure the constructive interference of the radiation diffracted from successive planes occurs if the Bragg' law is satisfied [101-104]:

$$2d_{hkl} \cdot \sin\theta_{hkl} = n\lambda \tag{4.1}$$

where d_{hkl} is the distance between crystal planes labelled by Miller indices (hkl), λ is the wave length of the incident x-ray beam, θ is the angle of incidence, and n is an integer. For certain θ value, the reflection from all parallel planes gives a strongly diffracted beam, presented as a Bragg peak in the XRD pattern. The positions and intensities of characteristic peaks are related to the crystal structure. The intensity of any diffraction peak in crystal structure is determined by many factors. Most important is the atomic scattering factor, f_α, which determines the scattering strength of an atom or ion. It increases as Z^2, with Z the number of electrons.

For all crystal structures with more than one atom or ion in the unit cell, additionally to the Bragg condition the structure factor, F_{hkl}, has to be considered [103]:

$$F_{hkl} = \sum_\alpha f_\alpha e^{-i\vec{G}_{hkl}\vec{r}_\alpha} \tag{4.2}$$

$$F_{hkl} = \sum_\alpha f_\alpha e^{2\pi i(hu_\alpha + kv_\alpha + lw_\alpha)} \tag{4.3}$$

where f_α is the atomic scattering factor, G_{hkl} the reciprocal lattice vector and r_α the real space vector of atom α in the unit cell.

The structure factor of face centred cubic lattice (fcc) with the simple cube as unit cell is [103]:

$$F_{hkl} = f(1 + e^{-i\pi(h+k)} + e^{-i\pi(h+l)} + e^{-i\pi(k+l)}), \tag{4.4}$$

resulting in the selection rules:

$$F_{hkl} = \begin{cases} 4f, & \text{h,k,l all even or odd} \\ 0, & \text{h,k,l mixed.} \end{cases} \tag{4.5}$$

In the fcc lattice no reflection can occur for which the Miller indices are mixed even and odd. The diffraction spectrum contains only peaks for which the indices that are all even or odd. For example, platinum and iridium have fcc crystal structure.

For diamond cubic structure (e.g. diamond, silicon, and germanium) the selection rules are [103]:

$$F_{hkl} = \begin{cases} 8f, & \text{h,k,l=4n all even (n=0,1,2…)} \\ 4\sqrt{2}, & \text{h,k,l all odd} \\ 0, & \text{h,k,l other combinations.} \end{cases} \tag{4.6}$$

For body centred cubic lattice (bcc), present in tantalum or chromium, the selection rules are [103]:

$$F_{hkl} = \begin{cases} 2f, & \text{h+k+l=even} \\ 0, & \text{h+k+l=odd.} \end{cases} \tag{4.7}$$

Identification of various crystalline compounds, or phases, is achieved by comparing the x-ray diffraction pattern from an unknown sample with a database of reference patterns (JCPDS) [105].

4.1.2 Atomic force microscopy

Surface roughness affects the function of a wide variety of engineering components. Perhaps the most demanding applications are in the optics and semiconductor industries. Atomic force microscopy (AFM) is one of the techniques suitable for imaging the surface and thus the measurement of surface roughness [106-109].

Atomic force microscopy (AFM) belongs to the group of scanning probe microscopy. AFM is based on the measurement of different forces (magnetic, electric, mechanical, and van der

Waals) between a sharp tip and the sample surface. Imaging is accomplished by measuring the interaction force (attractive or repulsive) via deflection of cantilever while scanning the tip across the surface.

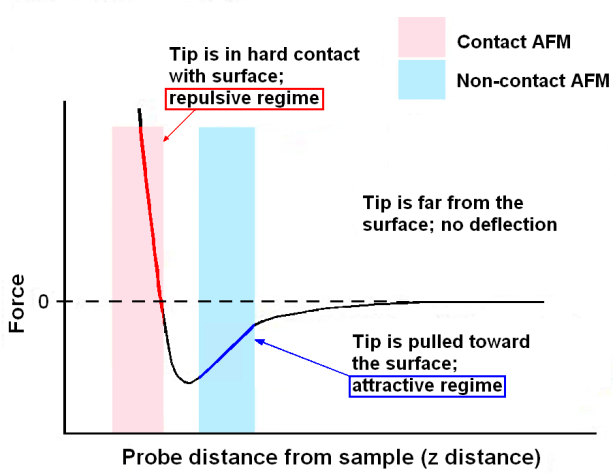


Figure 4.2 *Force-distance curve showing the interaction between probe tip and the sample surface.*

The interaction between tip and sample can be described by force distance curve (Figure 4.2) showing how the force changes when the sample approaches to the tip. At the large separation there is no interaction and the observed force is zero. As the sample is moved toward the tip, the tip is attracted due to the van der Waals interaction. If the sample is further moved to the tip, the total force acting on cantilever becomes repulsive.

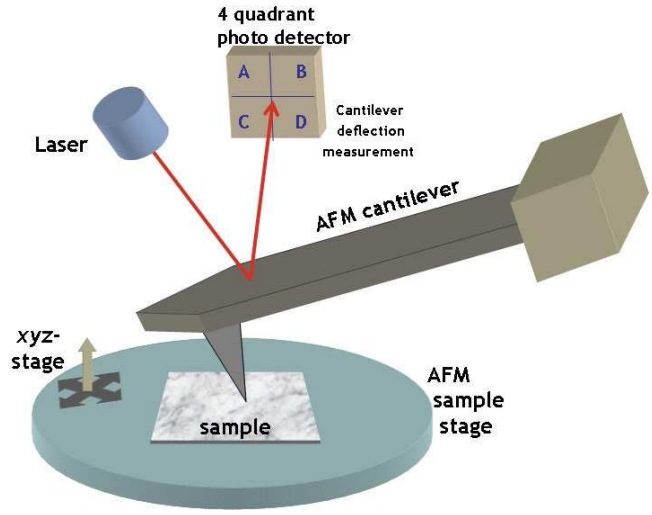


Figure 4.3 *The principle of AFM.*

The force acting on the tip is sensed by measuring the deflection of cantilever (Figure 4.3). The laser beam is focused and positioned on the cantilever surface. The reflected laser beam is directed towards a divided photodiode. As the cantilever deflection changes, the position of

reflected laser beam on the photodiode changes, and the difference between two positions is detected. Usually, the position of the tip is fixed and the sample is scanned. The lateral and vertical motion of the sample is preformed with a piezoelectric tube scanner.

The AFM can operate in contact, non-contact and tapping mode. In this work the roughness measurements were carried out on PICOStation (SIS, Herzogenrath) in non-contact mode. In non-contact AFM, a cantilever oscillates near its resonant frequency (100 kHz – 600 kHz) with very small amplitude (5 – 15 nm). The van der Waals attractive force between the tip and the sample acts upon the cantilever as the sample approaches to the tip, causing the shift in spring constant and thus the changes in amplitude (A_0) and the phase of the cantilever oscillations. The effective spring constant (k_{eff}) is:

$$k_{eff} = k_0 - \frac{\partial F}{\partial x} \tag{4.8}$$

Where k_0 is initial spring constant and $\partial F / \partial x$ is the force gradient. The spring constant affects the resonant frequency (f_0) of the cantilever:

$$f_0 = \sqrt{\frac{k_0}{m}} \tag{4.9}$$

The new frequency is given:

$$f_{eff} = \sqrt{\frac{k_{eff}}{m}} \text{ and } f_{eff} < f_0 \tag{4.10}$$

The oscillation amplitude (ΔA) decreases and reflects the distance change (Δd) between the probe tip and the surface. The topography is acquired using the feedback loop to compensate the distance change and make the oscillation amplitude (A_0) constant.

The root-mean-square roughness (*rms*) is the most widely used parameter for specification of the surface roughness. If the measured surface topography is represented as a surface profile *z(x)*, the *rms* roughness (*Rq*) is defined

$$Rq = \sqrt{\frac{1}{N-1}\sum_{j=1}^{N}\left(z_j - \bar{z}\right)^2} \tag{4.11}$$

where z_j is the surface profile and $\bar{z}$ the average roughness (R_a):

$$\bar{z} = \frac{1}{N}\sum_{j=1}^{N} z_j \tag{4.12}$$

The great analytical potential of AFM is based on a number of properties. In contrast to other surface analytical techniques, like e.g. scanning electron microscopy, AFM does not require vacuum. The insulators can be imaged without the need to coat them with a conductive film.

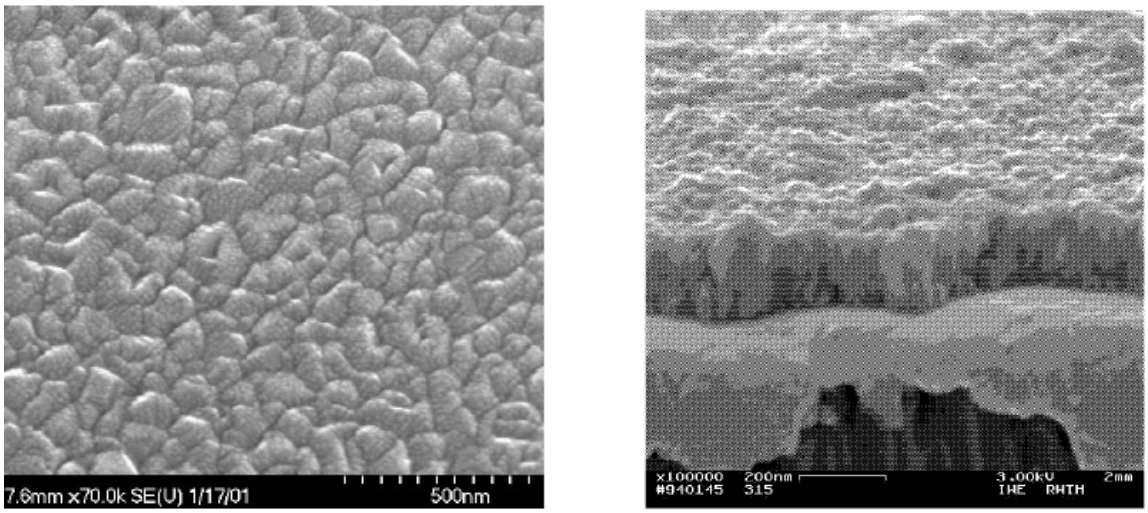
4.1.3 Scanning electron microscopy

Scanning electron microscopy (SEM) was performed to study the morphology of different films as a function of different processing parameters and thermal treatment at several temperatures. Both surface scans and cross sectional scans were made using Hitachi S-4100 field emission scanning electron microscope, with maximal magnification of 300 000 and resolution of 15 Å (at accelerating voltage 30 kV and working distance 5 mm).

For SEM operation high vacuum conditions ($< 10^{-4}$ Pa) are required in the specimen chamber [110, 111]. The electrons are accelerated from the electron source towards the sample with energies from 1 keV to 30 keV. The electron beam is focused onto the sample surface, causing the different interactions with specimen. The secondary electrons exit the sample near the surface (< 50 nm). The production of secondary electrons is topography related. Any changes in topography will change the yield of secondary electrons. For example, the edges emit more secondary electrons and thus appear brighter in the image. The backscattered electrons leave the specimen from a larger depth (up to 1 μm) and their emission depends on the atomic number, causes higher atomic number elements to appear brighter than lower atomic number elements. The electrons emitted from the sample surface are collected by a detector. The electron beam is scanned over the sample; the signal (emitted electrons) is collected by the detector and subsequently processed to generate the image.

The non-conducting samples, such as BTO and BST, can not dissipate the beam charges so that the charge accumulates on the surface. The associated electrical field causes the general distortion in the image, which leads to the lower image quality. Using lower accelerating voltages (< 5 kV), it is possible to reduce the charging effect and to get satisfying image resolution without a conducting coating on the samples surface.

The surface and the cross-section analysis with SEM enable the investigation of morphology and microstructure of thin film (Figure 4.4).



a) b)

Figure 4.4 *SEM image of 150 nm thick BST thin film made by a) CSD b) MOCVD.*

4.1.4 Rutherford backscattering spectroscopy

Rutherford backscattering spectroscopy (RBS) is one of the most frequently used techniques for quantitative analysis of composition, thickness, and depth profiles of thin solid films or solid samples near the surface region [106, 112-115].

The beam of monoenergetic ions, usually H^+ or He^+, with energies in the range 0.5 to 2.5 MeV, is directed at a sample surface. The energies of backward scattered ions are detected and analyzed (Figure 4.5a). In the backscattering collision, energy is transferred from the impinging particle to the stationary target atom. The energy ratio between the projectile energy E_1 after collision and the energy E_0 before collision, derived from binary collision theory, is:

$$\frac{E_1}{E_0} = K = \left[\frac{\left(M_2^2 - M_1^2 \sin^2\theta\right)^{1/2} + M_1 \cos\theta}{M_2 + M_1} \right]^2 \tag{4.13}$$

The energy ratio E_1/E_0 called the kinematic factor K, shows that the energy after scattering depends only on the mass M_1 of the projectile, the mass M_2 of the target atom, and the scattering angle θ (the angle between incident and scattered beams). If M_1, E_0, and θ are known, M_2 may be determined and the target element can be identified.

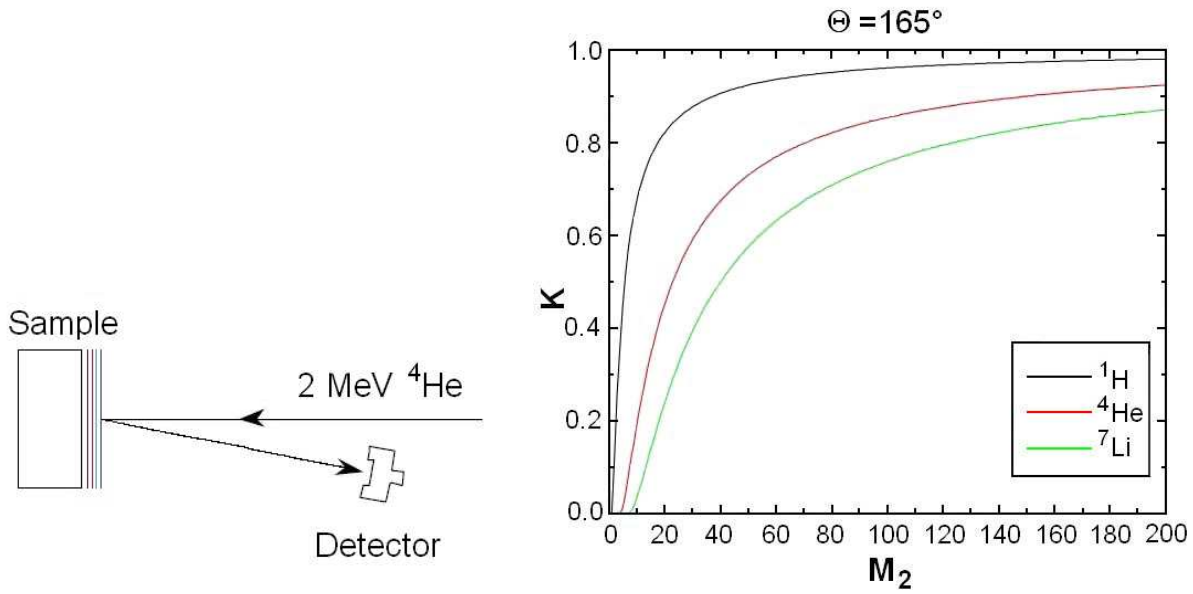


Figure 4.5 *a) Experimental setup for RBS and b) kinematic factor as a function of the target mass M_2 for incident H^+, He^+ and Li^+ ions at a scattering angle θ = 165° [116]*

For two different target elements with mass difference ΔM_2, the energy separation ΔE_1 of backscattered particles is given by:

$$\Delta E_1 = E_0 \frac{dK}{dM_2} \Delta M_2 \tag{4.14}$$

As can be seen from Figure 4.5b, the best energy separation and mass resolution are obtained for light target elements where the derivative dK/dM_2 is steep, while for heavy elements the mass resolution is small.

The energy of the backscattered ion given by (4.13) is only for scattering by an atom at the surface of the target. However, the ion beam penetrates the target in a straight line along witch the ions loose energy primarily through excitation and ionization of atomic electrons (electronic energy loss). The energy loss per unit path length, dE/dx, is called the stopping power. These energy losses broaden the peak to be observed in an RBS spectrum of a thin film and can be used for thickness (density/area) determination if the scattering species is known (Figure 4.6).

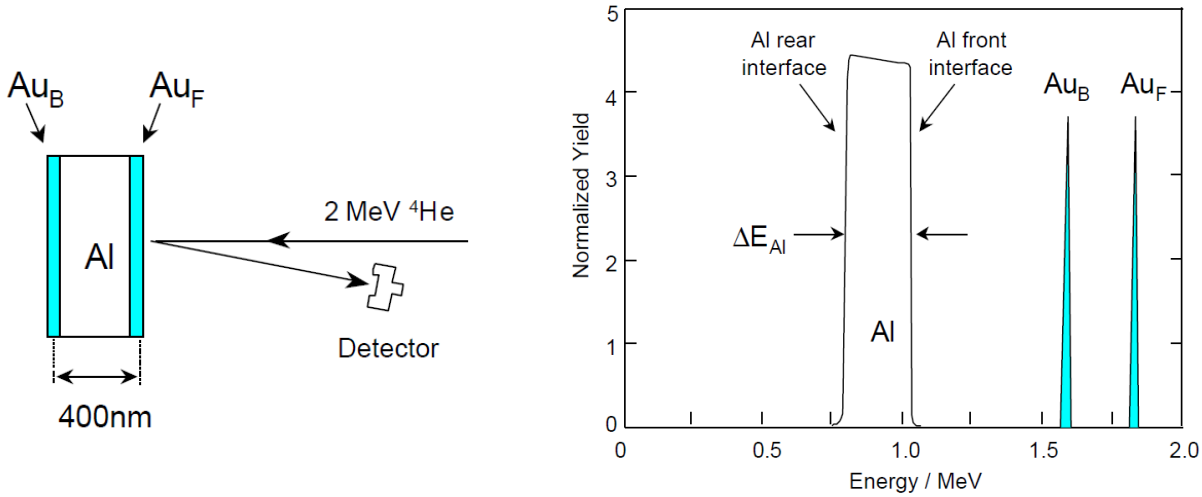


Figure 4.6 *Interpretation of the depth scale in RBS spectra.*

The energy difference, ΔE, for a particle scattered at the surface and a particle scattered at a depth x is given by:

$$\Delta E = [S] \cdot x \tag{4.15}$$

where *[S]*, called the energy loss factor, depends on the stopping power (*dE/dx*), kinematic factor *K* and the orientation of the sample to the incident beam and to the detector direction.

For surface analyses by RBS, conditions must be such that the mass of surface atoms is considerably higher than the mass of substrate atoms in order to resolve the peak from surface atoms. Otherwise, the peak from the surface layer merges with the broad continuum of substrate and appears as a small feature on top of it.

An RBS spectrum contains information about the mass of the scattering atoms, the composition of the surface layer, the depth of scattering atoms, and the thickness of a surface layer (Figure 4.6).

For an ion beam with the total number Q of ions impinging on a thin film, the number Q_A particles backscattered from atom types A and registered in the detector (also called yield Y_A) is given by:

$$Q_A = Y_A = QN_A\sigma_A\Delta\Omega \tag{4.16}$$

where N_A is the areal density of atoms A in the film (atom/cm^2), σ_A the differential scattering cross section-section, and $\Delta\Omega$ the angle of the detector. The composition of a film A_mB_n can be calculated from equation:

$$\frac{n}{m} = \frac{N_B}{N_A} = \frac{Q_B}{Q_A}\frac{\sigma_A(E,\theta)}{\sigma_B(E,\theta)} \tag{4.17}$$

A widely used RBS analysis program is the RUMP code [117]. The accuracy in RBS results is ~ 3 % for area densities and less than 1 % for stoichiometric ratios.

The real thin film density (d_{real}) can be calculated from areal density (N_A) knowing the thin film thickness:

$$N_A = t_{real,A} \cdot d_{real,A} \tag{4.18}$$

$$d_{real,A} = \frac{N_A}{t_{real,A}} \tag{4.19}$$

The thin film thickness could be measured using profilometer.

Ion beams suitable for RBS are produced in particle accelerator (in Institute of Solid State Research-IFF is used a 1.7 MeV Tandetron accelerator). To extract a beam suitable for material analysis, the beam is passed into the field of an analyzing magnet. A mass and charged selected beam then enters an UHV environment. The beam size at the target is typically 1 mm^2. The detection of backscattered ions is usually performed with a solid state detector, either a silicon surface barrier detector or a passivated implanted planar silicon detector. The detector signals, which are highly proportional to the energy of the incident particle, are amplified and assorted in energy in a multichannel analyzer.

4.1.5 X-ray fluorescence (XRF)

X-ray fluorescence (XRF) allows identifying and determining the concentration of elements present in solid, powder and films [110].

The x-ray beam impinges the sample material and high energy primary x-ray photons hit the atoms in the measured film. As a result, electrons from the inner orbitals are ejected in the form of photoelectrons converting the atoms into unstable ions. The missing electrons are replaced quickly by electrons from outer orbitals in order to restore a more stable atom state. These transitions are accompanied by an energy emission in the form of secondary x-ray photon (Figure 4.7). This phenomenon is known as fluorescence.

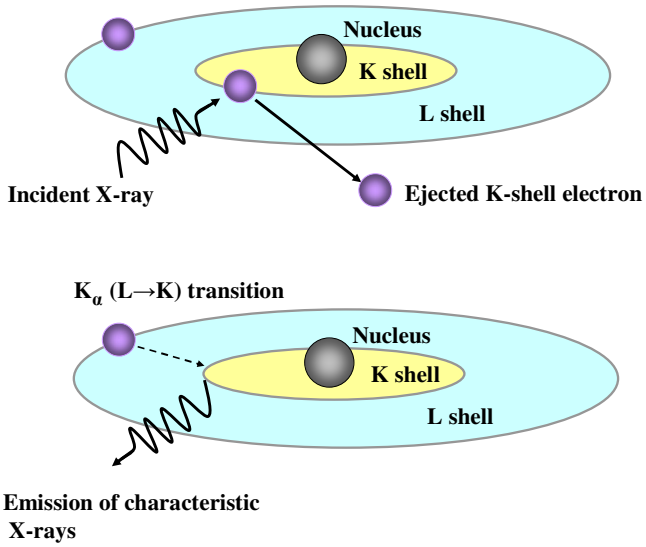


Figure 4.7 *Principle of fluorescence analysis*

The energy of emitted fluorescent photons can be calculated by the formula:

$$\Delta E = h \cdot \frac{c}{\lambda} \tag{4.20}$$

The energies and thus the wavelengths are characteristic for each element. It is possible to detect all different elements present in the sample by scanning over a wide 2θ spectrum, e.g. 10° – 90° (Figure 4.8). The lines are characteristic for the elements in the sample, while the background intensity level depends on the substrate. For the quantitative evaluation of the integral intensity the peak form can be considered as a pure Gaussian distribution (Figure 4.8).

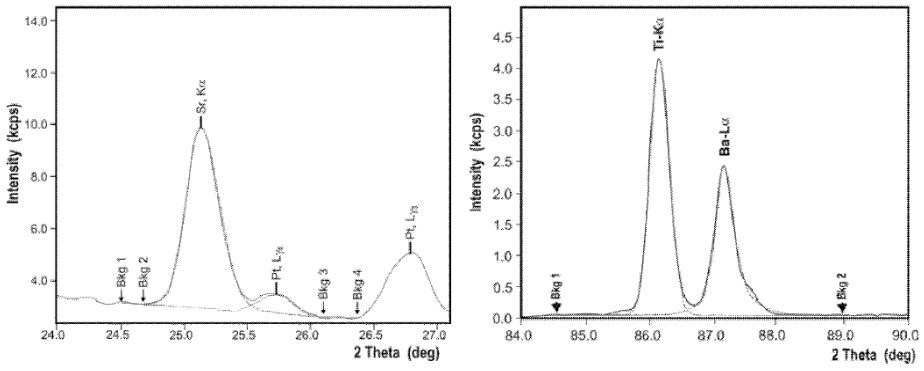


Figure 4.8 *Line spectrum of fluorescence analysis with background fitting and peak deconvolution a) Sr-K_α b) Ti-K_α and Ba-K_α.*

XRF analysis requires calibration samples and the evaluation of the results is always relative to the initial calibration.

4.2 Electrical characterization

4.2.1 Resistivity

The measurement of thin film sheet resistivity is frequently carried out using four-point probe method [118-120]. The four-point probe method can eliminate the effect introduced by contact, probe and spreading resistance. Two probes carry the current and the other two probes sense the voltage (Figure 4.9). Each tip is supported by springs on the other end in order to minimize sample damage during probing.

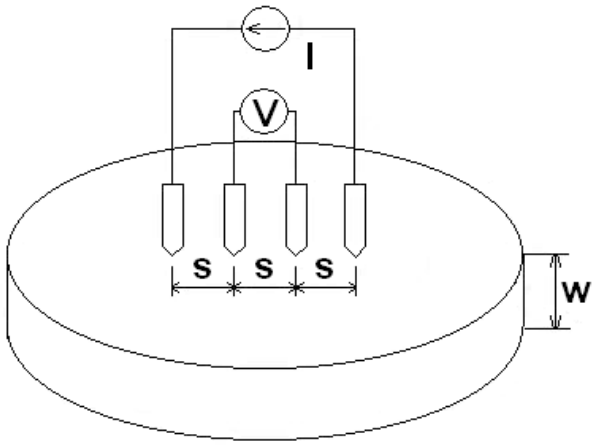


Figure 4.9 *Thin film sheet resistance measurement with four-point probe.*

The sheet resistance R_S of the thin homogenous film can be calculated:

$$R_S = \frac{V}{I} \cdot C\left(\frac{a}{d}, \frac{d}{s}\right) \tag{4.21}$$

where V is the voltage reading from voltmeter, I is the current carried by the two current carrying probes, C is a correction factor, s is the distance between the tips, a and d are sample length and width. For very thin samples with the probes being far from the sample edges the expressions of the sheet resistance becomes:

$$R_S = \frac{V}{I} \cdot \frac{\pi}{\ln 2} = 4.5324 \cdot \frac{V}{I} \tag{4.22}$$

For an infinite sample of finite thickness w the resistivity can be calculated:

$$\rho = \frac{V}{I} \cdot \frac{\pi}{\ln 2} \cdot w \cdot F\left(\frac{w}{s}\right) \tag{4.23}$$

where F is correction factor which approaching unity for $w/s < 0.4$.

In setup used in this work, the distance between tips is $s = 0.625$ mm and the thickness of measured films is in the order of magnitude $w \sim 10^{-7}$ m, and the ratio $w/s \sim 10^{-5}$. The resistivity of thin film can be calculated:

$$\rho = \frac{V}{I} \cdot \frac{\pi}{\ln 2} \cdot C \cdot w \tag{4.24}$$

4.2.2 Leakage current

Conductivity is an important characteristic value of electroceramic materials. It depends on the mobility of free electrons or ions charges in the material under the given conditions (e.g. temperature and applied electric field). The concentration of charge carriers is of crucial importance. An applied voltage results in a (leakage) current flow through the sample [86].

If ceramic capacitor is measured under DC voltage, the time dependent current or relaxation current follows a time-dependence known as Curie-von Schweidler behaviour and drops with an empirical power law [121]:

$$J(t) \propto t^{-n} \text{ with } 0.5 \leq \mathrm{n} \leq 1 \tag{4.25}$$

The regime of constant leakage current follows when the relaxation current is declined below the leakage current level. This is recognized as a plateau in the $logJ-logt$ plot as $J_L = \text{const}$ (Figure 4.10). The duration of leakage regime and consequently the beginning of the degradation behaviour cannot be exactly predicted and depends on the material itself and the external conditions, e.g. temperature and applied field [122-130]. The degradation is expressed in the rise of the "leakage" current under DC bias and is often followed by a dielectric breakdown.

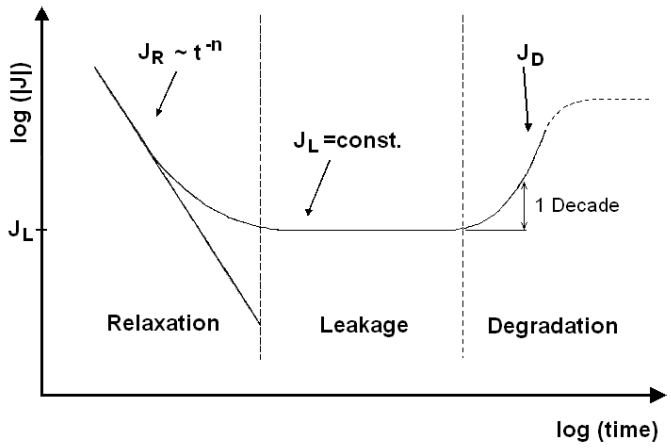


Figure 4.10 *Current response of a ceramic capacitor displaying typical behavior during DC load [123].*

The leakage current investigations were performed with a setup consisting of a voltage source Burster 4462 and a Keithley 617 electrometer, which are connected to the sample as shown in Figure 4.11, so that the positive voltage is applied to the top electrode. The Keithley electrometer has a minimum detection range of around 50 fA.

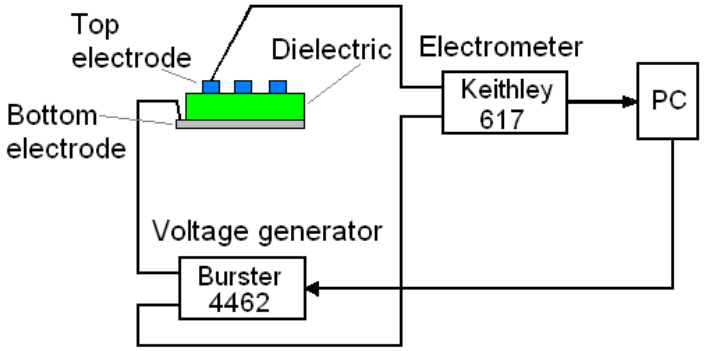


Figure 4.11 *The measurement setup used for the leakage current investigation.*

The leakage current dependence on applied voltage/electrical field is investigated by applying a special staircase-shaped voltage and measuring the current response (Figure 4.12). After each voltage step (V_s) the current acquisition follows for the desired time interval t_s until the relaxation effects have no influence on the leakage current.

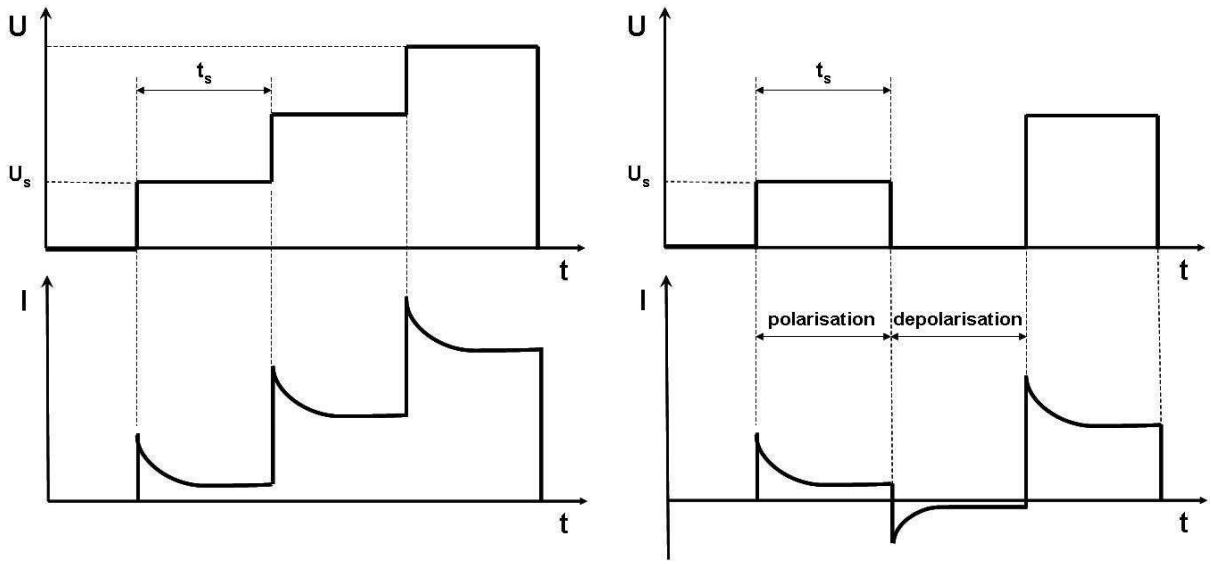


Figure 4.12 *Voltage staircase and the current response vs. time for situation a) without depolarization and b) with depolarization.*

The number of steps and the step height define the maximum applied voltage, which is set appropriate in order not to reach the breakdown limit. After polarization, a depolarization step may follow, where the voltage is set back to zero and the current is recorded. In this way it is controlled, whether there is any changes in relaxation current response [126].

4.2.3 Permittivity and loss tangent

The permittivity ε_r and loss tangent $tan\delta$ of the thin film capacitor where determined by measuring the capacitance at different bias voltages with the precision LCR meter HP 4284A from Hewlett Packard. Four terminal pair configuration is employed in order to exclude any mutual interference of the measurement signal and cables (Figure 4.13).

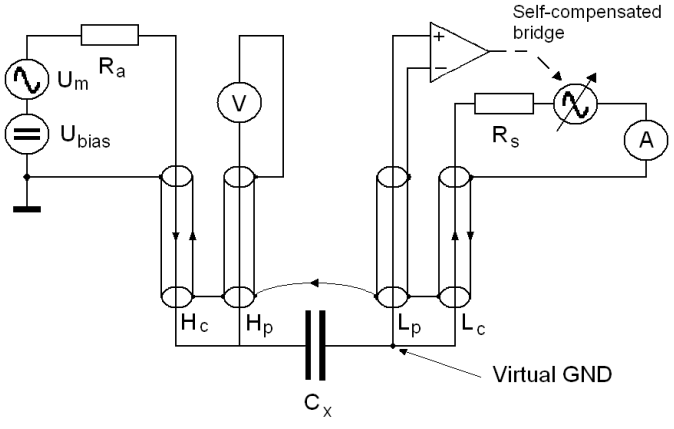


Figure 4.13 *Measurement principle of the HP4248A LCR bridge [131]. The unknown capacitance is labelled as C_x.*

The accurate measured value is obtained using instrument's compensation function. Two kind of compensation function are provided: open/short or open/short/load compensation, which eliminates the effects of the test fixture residuals, and cable length compensation, which minimizes the test port extension induced error [131]. As a result, a variety of error sources (such as residual impedance, admittance, cable length, etc.) can be eliminated.

The impedance analyzer allows to apply alternating voltage with a measurement frequency from 20 Hz up to 1 MHz, while the amplitude of small signal voltage U_m can be varied from 10 mV up to 1 V. An additional DC voltage bias U_{bias} can be superimposed on the small measuring signal, where U_{bias} ranges from –40 V up to 40 V. The potential drop U_x across the measured probe is equal:

$$\left|U_X\right| = \frac{\left|Z_X\right|}{\left|R_a + Z_X\right|} \cdot \left|U_{bias} + U_m\right| \tag{4.26}$$

where R_a is the source resistance (R_a=100Ω) and Z_x the probe impedance.

The standard characterization was preformed using an amplitude of $U_m = 50$ mV and measurement frequency 1 kHz, in order to avoid low frequency (50 Hz) interference with the power supply voltage (220 V) and high frequency stray fields.

The capacitance of the probe C_X is calculated:

$$C_X = \frac{1}{U_{bias} + U_m} \int I \cdot dt \tag{4.27}$$

The lateral dimensions of the samples, e.g. circular electrodes with diameter 0.1 – 1 mm, are many orders of magnitude larger then the thickness of dielectric material d (~ 100 nm) and can be considered as ideal planar capacitors. The relative permittivity of sample ε_r is then:

$$\varepsilon_r = \frac{C_X \cdot d}{\varepsilon_0 \cdot A} \tag{4.28}$$

The following equation shows the definition of the dissipation factor ($tan\ \delta$), which is the ratio of the imaginary part of the permittivity to the real part:

$$\tan\delta = \frac{\mathrm{Im}(\varepsilon_r)}{\mathrm{Re}(\varepsilon_r)} = \frac{\varepsilon_r''}{\varepsilon_r'} = \frac{1}{2\pi f C_X R_X} \tag{4.29}$$

$$\varepsilon_r = \varepsilon_r^{'} - j\varepsilon_r^{''} = \frac{d}{\varepsilon_0 A}\left(C_X - j\frac{1}{2\pi f R_X}\right) \tag{4.30}$$

The capacitance measurement of ceramic thin film as a function of the bias voltage or applied electric field gives so called *C(V)* or *C(E)* characteristic. It is often plotted as permittivity-voltage curves, so that the curves are independent from the capacitor geometry, thickness and can be easily compared to each other. Field dependent permittivity is significant at higher electric fields and its behaviour depends on variety of factors, such as deposition technique, temperature, thickness, electrode material [13, 14, 87, 88, 132-136].

4.2.4 Ferroelectric properties

The electrical characterization of ferroelectric materials is crucial to investigate their suitability for different applications. Typical measurement is the hysteresis curve of electric polarization [86, 137]. To obtain the dynamic hysteresis loop of a ferroelectric capacitor the polarization is measured versus applied voltage (Figure 4.14).

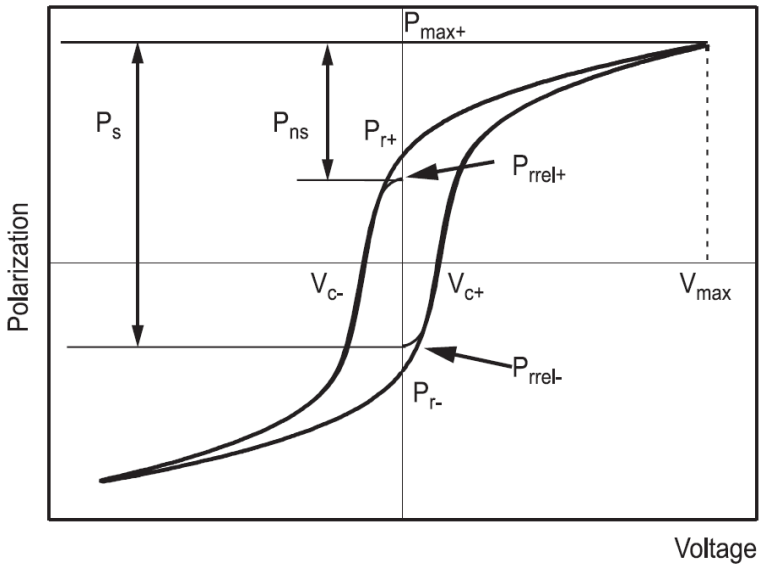
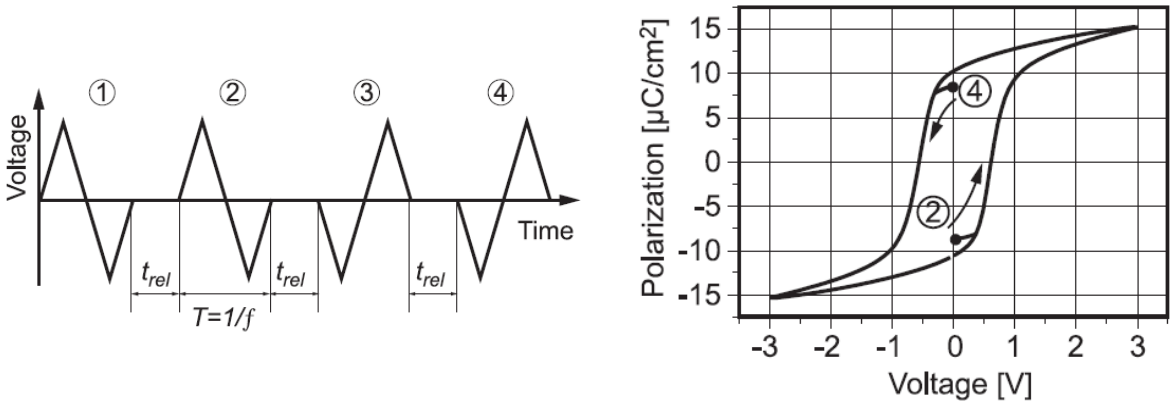


Figure 4.14 *Hysteresis loop with nomenclature of characteristic values [137].*

To have a standardized and comparable hysteresis loop, certain parameters are commonly fixed (Figure 4.15a). The pre-polarization pulse 1 establishes a defined polarization state, the negative state of relaxed remanent polarization after 1 second. The hysteresis loop corresponding to pulse 2 starts at the negative relaxed remanent polarization state P_{rrel-} and turns into the positive saturation P_{max+} (Figure 4.15b). The third loop establishes the sample into the positive remanent polarization state P_{r+} without sampling data. The fourth loop now

starts in the positive relaxed remanent polarization state P_{rrel+}, turns into negative saturation P_{max-}.



a) b)

Figure 4.15 *a) The voltage pulse applied on the ferroelectric sample during hysteresis measurement b) Exemplary hysteresis loop [137].*

The shape of hysteresis curve changes with frequency, amplitude and relaxation time between pre-polarization and recording pulses of the excitation signal and depends on the thin film characteristics [138-141].

The hysteresis curves presented in this work were recorded with an aixACCT TF analyzer. Hysteresis measurement can be performed in dynamic range of 1 Hz up to 2 kHz, while the maximum output voltage is limited to 10 V.

5 Experimental results and discussion

The tantalum silicon nitride alloys (TaSiN) are ternary mixtures. As long as the amorphous phase occurs, TaSiN is free of fast diffusion paths (such as grain boundaries) and thus, suitable for use in oxygen diffusion barrier applications. The properties of these alloys depend on the composition: a high concentration of tantalum creates low resistivity, a high concentration of silicon induces oxidation resistance whereas a high concentration of nitrogen increases the temperature of crystallization. In this work, the composition and structure of TaSiN thin films used as oxygen diffusion barriers were optimized in order to prevent the oxidation of highly doped silicon substrate under high temperature conditions while remaining electrically conductive.

5.1 Properties of tantalum silicon nitride thin films

5.1.1 Stoichiometry dependence on the deposition parameters

Thin films of TaSiN with differing compositions were deposited by radio frequency (rf) reactive magnetron sputtering in a high vacuum system Leybold Univex 450B using two Ta-Si targets with different compositions. The targets measured 4" in diameter and 2 cm thick. The composition of the targets was determined using Rutherford backscattering spectroscopy (RBS). The RBS data were evaluated with a commercially available RUMP program. Figure 5.1 illustrates the measured and simulated data for two different Ta-Si targets. Since the Si atoms have a lower mass than the Ta atoms, the kinematic factor for Si atoms is less than that of the Ta atoms ($K_{Si} < K_{Ta}$). Using equation (5.1), derived from binary collision theory [106]:

$$\frac{E_1}{E_0} = K = \left[\frac{\left(M_2^2 - M_1^2 \sin^2 \theta\right)^{1/2} + M_1 \cos\theta}{M_2 + M_1} \right]^2 \tag{5.1}$$

with a scattering angle $\theta = 173°$ and a beam energy of $^4He^+$ ions, $E_0 = 1.405$ MeV, the values of the kinematic factor for tantalum and silicon are:

$$K_{Ta} = 0.9157 \text{ and } K_{Si} = 0.5647 \tag{5.2}$$

The energies of backscattered ions by tantalum and silicon atoms at target surface are:

$$E_{Ta} = 1.29 \text{ MeV and } E_{Si} = 0.793 \text{ MeV}, \tag{5.3}$$

respectively.

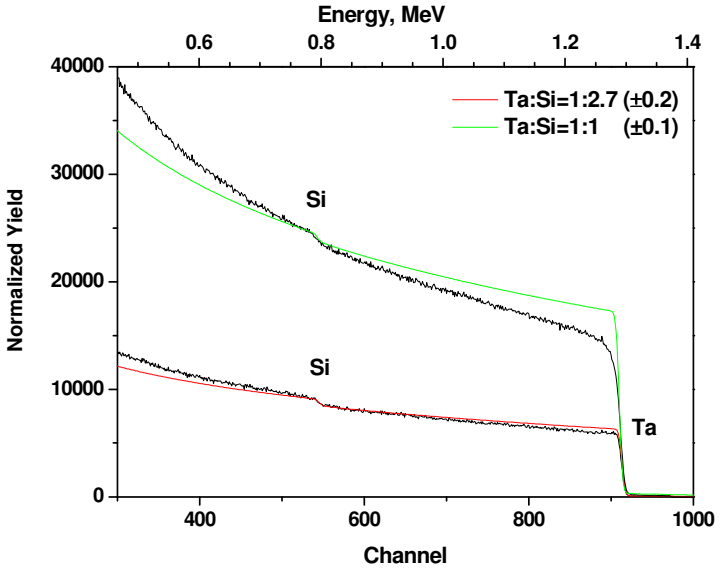


Figure 5.1 *RBS diagram for two Ta-Si targets with different compositions.*

Backscattered $^4He^+$ ions originating from the Ta atoms appear at higher energy in the spectrum. Very broad spectra and the absence of any peak indicate that the target has the infinite depth (for RBS greater than 1 μm). The agreement between the simulation and measured data is acceptable, and the ratio of tantalum to silicon could be obtained. The ratios of Ta to Si in the targets are 1:1 and 1:2.7 with the deviation of ± 0.1 and ± 0.2, respectively. The results correspond to compositions of TaSi and Ta_2Si_5.

The composition of TaSiN thin films was varied by means of the power supply to the Ta_2Si_5 target. The base pressure of the vacuum system was $7 \cdot 10^{-7}$ mbar. The total gas pressure during the sputtering was 10^{-2} mbar. The total gas flow rate (60 sccm) as well as the ratio of nitrogen to argon was kept constant (6 sccm N_2 + 54 sccm Ar) during sputtering. Before the initiation sputtering the vacuum chamber was flushed with nitrogen gas for 600 s. While the

shutter was closed, the target was pre-sputtered for 60 s before each deposition. The deposition temperatures were 300 °C and 500 °C (Appendix A.2, Table A.2.1).

Stoichiometry and thickness of TaSiN films were determined by 1.405 MeV He^+ RBS random spectra. For the RBS measurements the substrate was a (100)-oriented, highly boron doped p^{++}-silicon wafer. Before deposition, the silicon substrate was etched in 40 % hydrofluoric acid (HF) for 10 seconds in order to remove the native silicon-dioxide. After that it was rinsed in deionised water and dried in a nitrogen gas stream. For resistivity measurements TaSiN thin films were deposited on insulating Si/SiO_2 substrate.

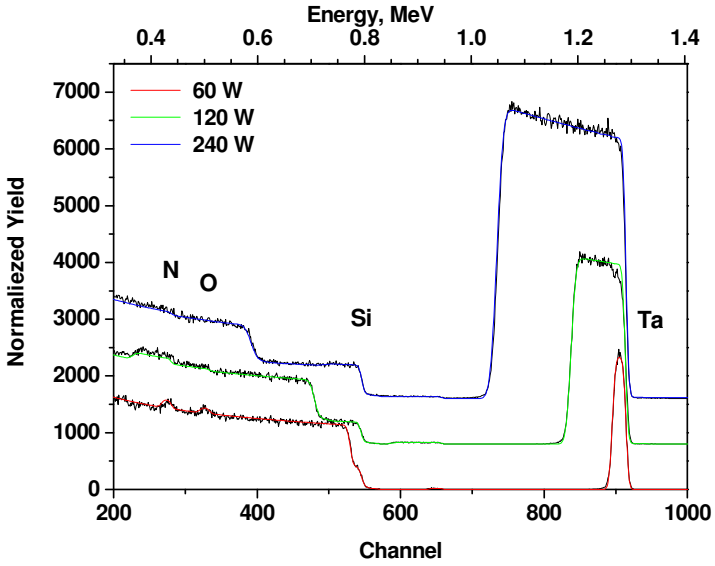


Figure 5.2 *RBS spectra of TaSiN layers deposited with different target power at 500 °C for sputtering gas Ar + 10 % nitrogen.*

Oxygen contamination was confirmed from the RBS spectra (Figure 5.2) and analysed by fitting experimental data. The summary is presented in the Table 5.1. The TaSiN stoichiometry is expressed in atomic percent. The energies of backscattered ions by oxygen and nitrogen atoms at target surface are: E_O = 0.508 MeV and E_N = 0.436 MeV.

Table 5.1 *TaSiN stoichiometry dependence on deposition parameters.*

Target Ta:Si	Power, [W]	T, [°C]	Sputter rate, [Ås^{-1}]	Stoichiometry	Ta:Si (film)	Si:N (film)
1:2.7	60	500	1.4	$Ta_8Si_{27}N_{43}O_{21}Ar_1$	1:3.4	1:1.6
	120	300	4.7	$Ta_{13}Si_{36}N_{43}O_7Ar_2$	1:2.8	1:1.2
	120	500	5.1	$Ta_{12}Si_{35}N_{42}O_9Ar_2$	1:2.9	1:1.2
	240	300	9.7	$Ta_{19}Si_{55}N_{22}O_2Ar_2$	1:2.9	2.5:1
	240	500	9.4	$Ta_{19}Si_{56}N_{21}O_2Ar_1$	1:2.9	2.7:1

The sheet resistance measurement using 4 point probe technique shows that all layers are insulating ($R > 10^6$ Ω). It is attributed to the oxygen content in the TaSiN layers. Decreasing the target power increases the nitrogen and oxygen content in the layers. The contamination with oxygen could possible arise through the pipe line for the sputter gas, which had also been used in other experiments for reactive sputtering in oxygen.

In all the following experiments, the sputter gas consisted of a prepared gaseous mixture containing 1 % N_2 and 99 % Ar. This mixture was introduced in the vacuum chamber through a separate pipe line. As in the previous sets the gas flow rate was kept constant (6 sccm of gas mixture 1 % N_2 + 99 % Ar and 54 sccm Ar). If flushing time lasted less then 600 s, the TaSiN layers became contaminated with oxygen. The deposition temperature was room temperature (RT). For the resistivity measurements TaSiN thin films were deposited on insulating Si/SiO_2 substrate. In order to estimate the density of as-deposited TaSiN thin films, the layer thickness was measured using the surface profiler Veeco DEKTAK 3. All as-deposited TaSiN layers have a metallic grey colour and a smooth mirror-like appearance.

Then using different targets the influence of applied power on the stoichiometry of the TaSiN thin films was investigated (Table A.2.2). Figure 5.3 demonstrates the simulation of the TaSiN stoichiometry in as-deposited thin films as well as the thickness derived from RBS measurement for the different layers.

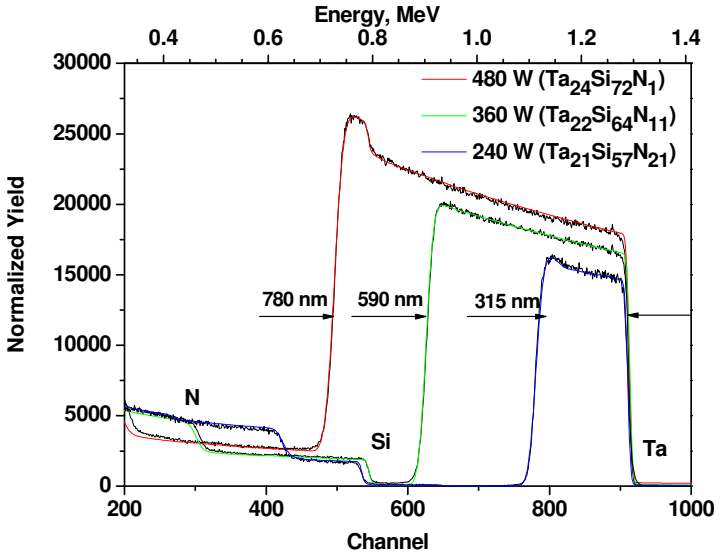


Figure 5.3 *Representative RBS diagrams for TaSiN layers on silicon substrate.*

Table 5.2 summarises the sputter parameters, the stoichiometry, the density and the ratio of tantalum to silicon and of silicon to nitrogen in as-deposited TaSiN thin films for the different sputter targets. The deviation of the element composition is ± 1. Along with the nitrogen, a

small amount (1 %) of argon sputter gas was incorporated in the TaSiN thin films. The amount of argon increases with increasing sputter power to about 3 %.

The ratio of Ta to Si depends on their ratio in the target and remains constant with different sputter power. Increasing the power decreases the nitrogen content in the thin films. The ratio of tantalum to nitrogen is independent on the different sputter targets using the same sputter power.

Table 5.2 *TaSiN stoichiometry dependence on deposition parameters*

Target Ta:Si	Power, [W]	Sputter rate, [Ås^{-1}]	Stoichiometry	Ta:Si (film)	Ta:N (film)	d, gcm^{-3}
1:2.7	120	4	$Ta_{15}Si_{44}N_{41}Ar_1$	1:2.9	1:2.7	3.26
	180	6.5	$Ta_{19}Si_{54}N_{26}Ar_1$	1:2.8	1:1.4	4.65
	240	7.3	$Ta_{21}Si_{57}N_{21}Ar_1$	1:2.7	1:1	3.83
	360	13.2	$Ta_{22}Si_{64}N_{11}Ar_3$	1:2.9	2:1	4.94
	480	17.6	$Ta_{24}Si_{72}N_1Ar_3$	1:3.0	24:1	5.46
1:1	120	1.3	$Ta_{22}Si_{22}N_{54}Ar_1$	1:1	1:2.5	6.30
	180	2.1	$Ta_{28}Si_{28}N_{43}Ar_1$	1:1	1:1.5	7.98
	240	3.5	$Ta_{33}Si_{33}N_{33}Ar_1$	1:1	1:1	7.19

As expected the sputter deposition rate was greater for higher sputter power (Figure 5.4). The sputter yield increases roughly linearly with sputter power, i.e. incident argon ion energy, for both targets.

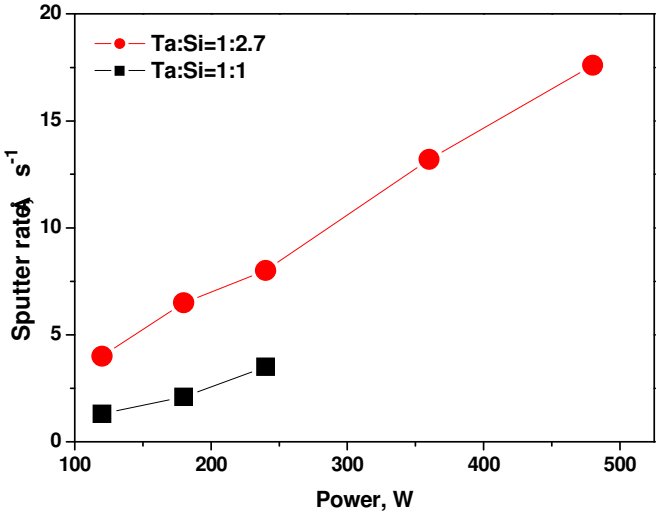


Figure 5.4 *Sputter rate versus sputter power for two targets with different ratios of Ta to Si for sputtering gas Ar + 1 % N_2 at room temperature.*

The sputter deposition rate for the Ta_2Si_5 target is greater and the density of as-deposited TaSiN layers is lesser than for the TaSi target (Figure 5.5). In contrast to the denser TaSiN gained from the TaSi target, the TaSiN thin films obtained from Ta_2Si_5 target are porous. The same dependence for density was found for the different target powers. The film density was estimated from the TaSiN atomic density (at cm^{-2}) determined by RBS whereas the film thickness was measured with the surface profiler.

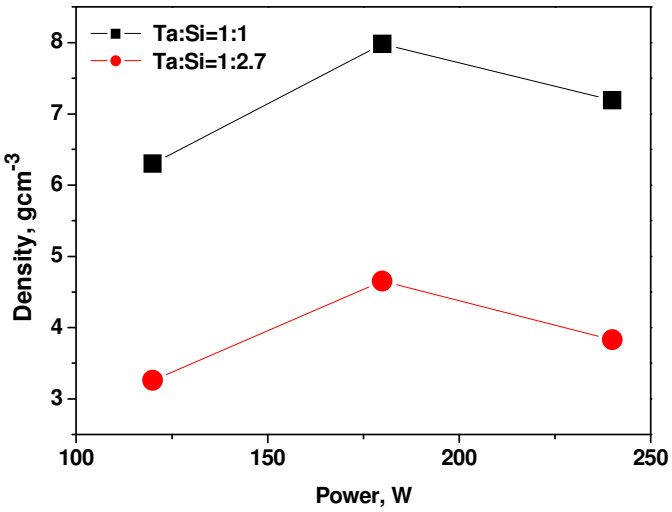


Figure 5.5 *TaSiN thin film density as a function of sputter power for the two different sputter targets.*

In order to optimize the deposition parameters, the influence of the deposition temperature was investigated. There was no difference in stoichiometry for the films deposited at room temperature and at 500 °C (Table 5.3). The resistances differ slightly. Therefore, room temperature was set as the standard deposition temperature.

Table 5.3 *Stoichiometry independence of TaSiN on deposition temperature.*

Target Ta:Si	Power, [W]	Temperature	Stoichiometry	Resistivity, [Ωm]
1:2.7	240	Room temperature	$Ta_{21}Si_{57}N_{21}Ar_1$	$1.5 \cdot 10^{-5}$
	240	500 °C	$Ta_{22}Si_{57}N_{20}Ar_2$	$9.2 \cdot 10^{-6}$

The different TaSiN layer compositions which were obtained by sputter deposition are represented in the ternary phase diagram (Figure 5.6). The diagram is presented as an equilateral triangle with pure elements at the corners, binary phases along the edges and ternary compositions in the interior. Figure 5.6 shows the TaSiN composition range {Ta (20 – 25 at %) – Si (20 – 45 at %) – N (35 – 60 at %)}, identified as optimum for use as

an oxygen diffusion barrier in stacked capacitor DRAM structures reported by Cabral et al. [6].

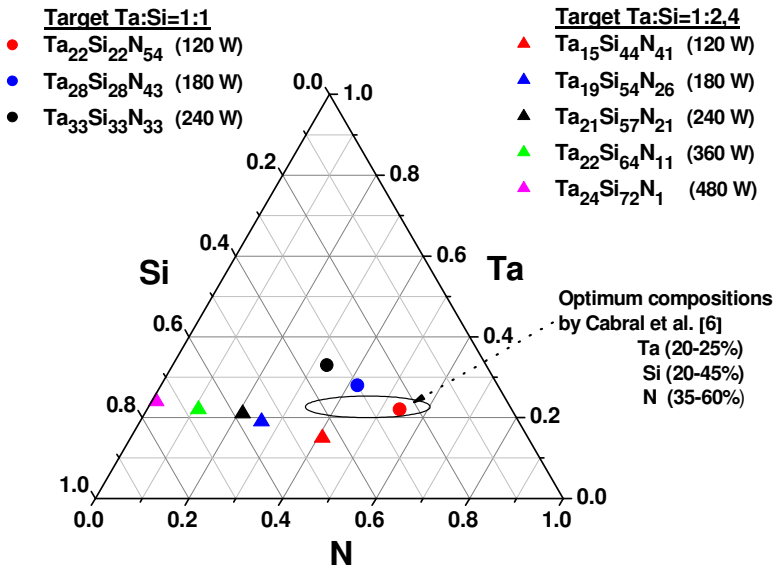


Figure 5.6 *Ternary phase diagram showing the TaSiN compositions (extracted by RBS) of thin films deposited by reactive RF magnetron sputtering.*

The TaSiN films should preferably remain amorphous after processing the dielectric thin film at 700 °C. The samples were annealed at temperatures above 700 °C using rapid thermal annealing (RTA) for 10 minutes in an oxygen atmosphere, with warm-up rate of 100 °C/s and a cool down rate of 50 °C. They were then analysed in terms of crystallinity determined by x-ray diffraction (XRD) in the conventional Bragg-Brentano ($\theta - 2\theta$) geometry and compared to results of the as-deposited TaSiN thin films (see Figure 5.7). Because of the interfering effect of the Si substrate, the glancing incident diffraction geometry, i.e. low angle of X-ray incident beam, was also used. The glancing angle was $\alpha = 1°$. The results are then plotted in Figure 5.7.

All TaSiN thin films with different compositions were amorphous after deposition and annealing at 700 °C. After annealing at 750 °C the $Ta_{21}Si_{57}N_{21}$ thin film crystallizes, and its structure appears to be polycrystalline and contains a $TaSi_2$ phase, as listed in Table A.1.1 (Appendix A.1).

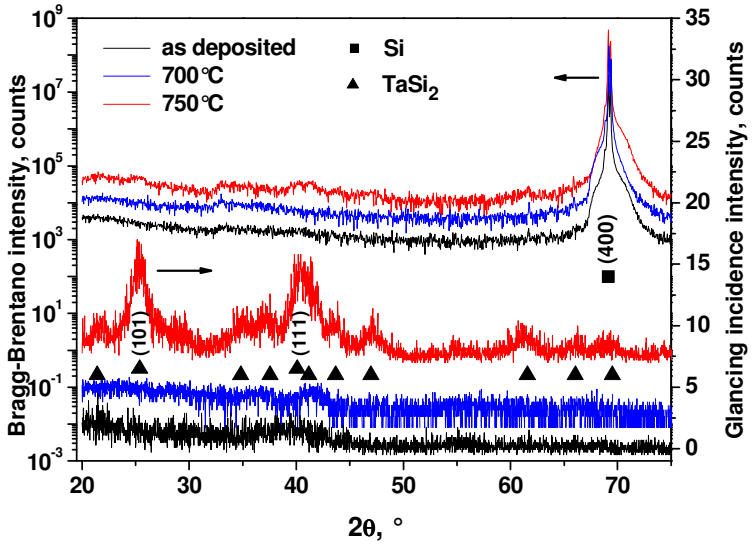


Figure 5.7 *θ-2θ and glancing incident spectra for $Ta_{21}Si_{57}N_{21}$ thin film as-deposited on (100)-oriented Si and after annealing at 700 °C and 750 °C for 10 minutes in oxygen atmosphere.*

The annealing temperature, at which the formation of $TaSi_2$ phase with hexagonal crystal structure occurs, was defined as crystallization temperature for TaSiN thin films (Table 5.4). The nitrogen content in the film influences the crystallization temperature and shifts it to the higher values. The films with a ratio of tantalum to silicon 1:1 crystallized also in the $TaSi_2$ phase.

Table 5.4 *Crystallization temperature[*] (T_{cryst}) for TaSiN with different compositions after annealing in oxygen for 10 min.*

TaSiN	T_{cryst}, [°C]
$Ta_{15}Si_{44}N_{41}$	900
$Ta_{19}Si_{54}N_{26}$	800
$Ta_{21}Si_{57}N_{21}$	750
$Ta_{22}Si_{22}N_{54}$	1000
$Ta_{28}Si_{28}N_{43}$	900
$Ta_{33}Si_{33}N_{33}$	800

[*] The crystallization temperature, T_{cryst}, is defined as the annealing temperature at which the formation of the $TaSi_2$ phase with hexagonal crystal structure occurs.

The crystallization temperature, T_{cryst}, increases with increasing nitrogen content in the TaSiN film (Figure 5.8). The slope for samples with a ratio of Ta to Si 1:1 is larger than that for the samples with a ratio 1:2.7.

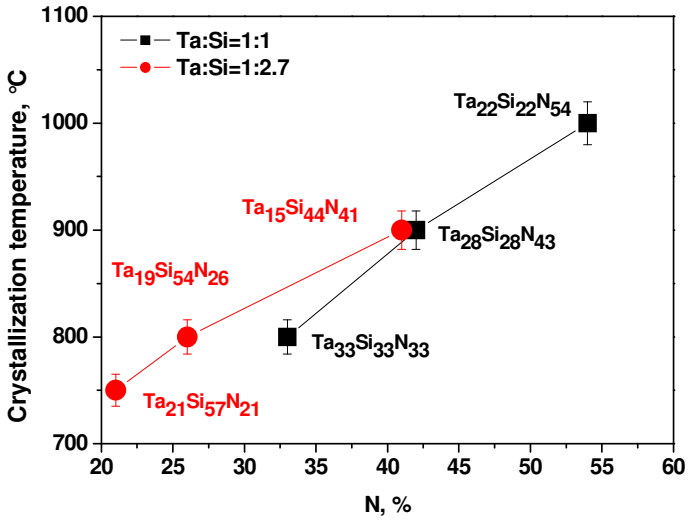
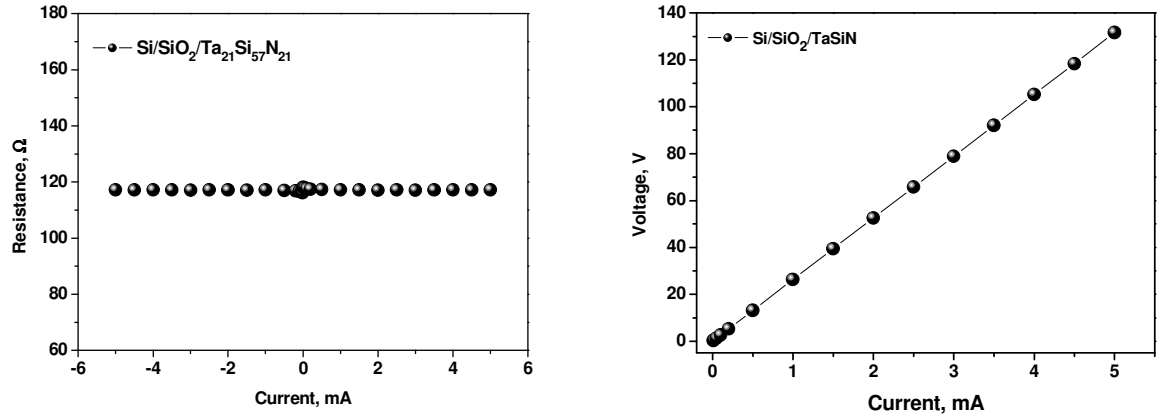


Figure 5.8 *Crystallization temperature dependence on nitrogen content for the different TaSiN compositions.*

5.1.2 Resistivity

TaSiN thin films should act as conductive diffusion barrier for highly doped p^{++}-silicon substrates, with boron doping density of $N_a = 10^{20}$ cm^{-3}. Furthermore, they should remain conductive after processing the high-κ dielectric material, usually deposited at 700 °C in oxygen atmosphere. Both annealing at a high temperature as well as the electrical characterization of as-deposited TaSiN thin film is crucial for the choice as a diffusion barrier. Using the four point probe method, the sheet resistance and resistivity of TaSiN films were determined. For the resistance measurement, the TaSiN thin films were sputtered on insulating Si/SiO_2 substrate at room temperature. The target and sputter varied in order to achieve the different compositions of TaSiN. The sputter gas was argon with 1 % nitrogen.
The TaSiN thin films have metallic conduction with ohmic behaviour, i.e. constant resistance or linear voltage to current dependence (Figure 5.9).



a) b)

Figure 5.9 *a) Sheet resistance and b) voltage-current dependence for $Ta_{21}Si_{57}N_{21}$ thin film.*

The resistivity of films with different TaSiN compositions is represented in the Table 5.5. In all cases, the ohmic behaviour was registered for as-deposited TaSiN thin films. The resistivity of TaSiN layers is two order of magnitude higher than the platinum resistivity ($1.1 \cdot 10^{-7}$ Ωm), which is satisfying for the purpose as a conductive oxygen diffusion barrier. Only the $Ta_{22}Si_{22}N_{54}$ sample had a resistance that was too high and therefore unacceptable.

Table 5.5 *Resistivity dependence on TaSiN stoichiometry.*

Target Ta:Si	TaSiN	Resistivity, [a] [Ωm]
1:2.7	$Ta_{15}Si_{44}N_{41}$	$8.8 \cdot 10^{-5}$
	$Ta_{19}Si_{54}N_{26}$	$1.7 \cdot 10^{-5}$
	$Ta_{21}Si_{57}N_{21}$	$1.5 \cdot 10^{-5}$
	$Ta_{22}Si_{64}N_{11}$	$9.0 \cdot 10^{-6}$
	$Ta_{24}Si_{72}N_{01}$	$5.0 \cdot 10^{-6}$
1:1	$Ta_{22}Si_{22}N_{54}$	$3.5 \cdot 10^{-3}$
	$Ta_{28}Si_{28}N_{43}$	$1.8 \cdot 10^{-5}$
	$Ta_{33}Si_{33}N_{33}$	$9.8 \cdot 10^{-6}$
	TaSi [b]	$2.5 \cdot 10^{-6}$
	[b] Sputter gas Ar	[a] Substrate Si/SiO_2

By increasing the tantalum content, resistivity decreases. In this study, the tantalum content in the TaSiN layers varies only slightly; therefore, this relationship could not be observed

clearly. However, the variation in the nitrogen content in the TaSiN layers is more pronounced as depicted in Figure 5.10. Increasing the nitrogen content increases the resistivity of as-deposited TaSiN thin films.

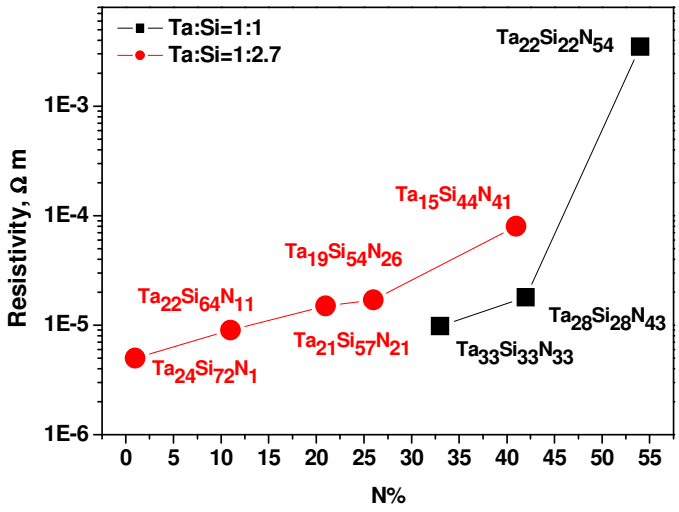


Figure 5.10 *Resistivity dependence on nitrogen content for the different TaSiN compositions.*

As mentioned earlier, when using TaSiN thin film as an oxygen diffusion barrier, it has to remain conductive after the deposition of the high κ dielectric material at high temperatures in oxygen atmosphere. Therefore one of the most important parameters for TaSiN thin films is the resistivity after processing of dielectric thin film at 700 °C. The TaSiN thin films on insulating Si/SiO_2 substrate were annealed in the RTA at 700 °C for 10 minutes in oxygen atmosphere. Their resistance after annealing is summarised in Table 5.6.

Table 5.6 *Resistivity before and after annealing in O_2 at 700 °C for 10 min for different TaSiN compositions.*

TaSiN	ρ, [Ω] (as-deposited)	ρ, [Ω] (after 700 °C)
$Ta_{15}Si_{44}N_{41}$	$8.8 \cdot 10^{-5}$	$3.8 \cdot 10^{-5}$
$Ta_{19}Si_{54}N_{26}$	$1.7 \cdot 10^{-5}$	$2.0 \cdot 10^{-5}$
$Ta_{21}Si_{57}N_{21}$	$1.5 \cdot 10^{-5}$	$1.4 \cdot 10^{-5}$
$Ta_{22}Si_{22}N_{54}$	$3.5 \cdot 10^{-3}$	Not conductive
$Ta_{28}Si_{28}N_{43}$	$1.8 \cdot 10^{-5}$	Not conductive
$Ta_{33}Si_{33}N_{33}$	$9.8 \cdot 10^{-6}$	$1.3 \cdot 10^{-5}$

The layers that had higher nitrogen and lower silicon content had insulating properties following the annealing process. This result could possibly be due to the formation of an oxide layer. It has been reported that the thickness of the oxide layer on TaSiN films depends on silicon content [9]. The oxygen penetration depth into TaSiN layer decreases as the silicon composition increases. The samples with the same nitrogen content but higher silicon content show better oxidation resistance and thus remain conductive after annealing at 700 °C.

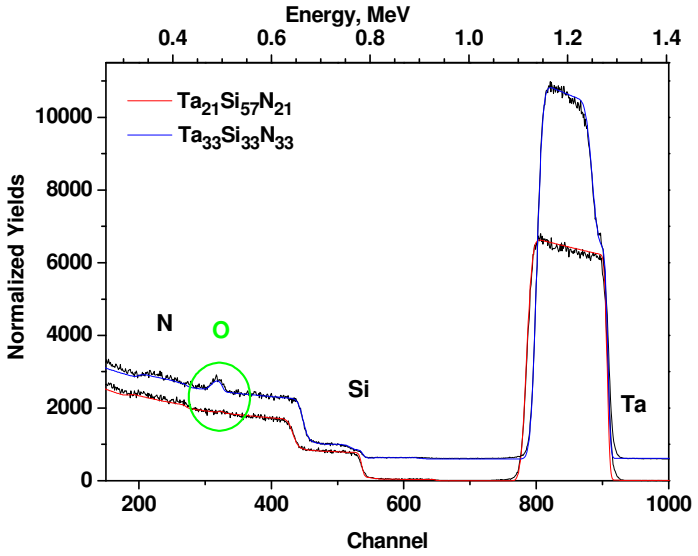


Figure 5.11 *RBS diagram for the $Ta_{21}Si_{57}N_{21}$ and $Ta_{33}Si_{33}N_{33}$ layers on the silicon substrate after annealing at 700 °C in an oxygen atmosphere*

Figure 5.11 illustrates the measured and simulated RBS data (black and coloured curves, respectively) for Si/$Ta_{21}Si_{57}N_{21}$ and Si/$Ta_{33}Si_{33}N_{33}$ samples after annealing at 700 °C. An oxidized $TaSiN_xO_y$ layer is clearly present at the top of the TaSiN thin films after annealing. The thickness of these layers is estimated to be about 5 nm for $Ta_{21}Si_{57}N_{21}$ and 35 nm for $Ta_{33}Si_{33}N_{33}$, respectively. The absence of an oxidized layer at the Si/TaSiN interface indicates that the TaSiN is an excellent barrier to oxygen diffusion. However, a lower-temperature processing or an improved electrode/barrier material is needed if the oxidized $TaSiN_xO_y$ material has a high resistance.

5.1.3 Influence of the substrate

The objective of this work is to produce the conductive oxygen barrier on highly doped p^{++}-silicon substrate. The silicon substrate was etched in 40 % hydrofluoric acid (HF) in order to remove native silicon-dioxide, then rinsed in deionised water, dried in nitrogen stream and immediately transferred into a vacuum chamber with a base pressure $1 \cdot 10^{-7}$ mbar. TaSiN thin films were sputtered directly on (100)-oriented silicon substrate. The sputter parameters have been previously described in detail. In order to achieve the different TaSiN

stoichiometry, the target power was varied, while the deposition temperature (room temperature) and sputter gas (Ar + 1 % N_2) remained constant.

A metal to semiconductor junction can behave either as a Schottky barrier or as an ohmic contact, depending on characteristics of the material itself and interface between them. Ohmic contact is defined as a metal-semiconductor contact that has negligible contact resistance, i.e. the voltage drop across the interface is small compared with a drop across the semiconductor.

Silicon substrate and TaSiN layer in Si/TaSiN stack are in parallel connection when measured using the 4 point probe sheet resistance method (see Figure 5.12), and in the case of low contact resistance between them, the equivalent resistance is given by the equation:

$$\frac{1}{R_e} = \sum_i \frac{1}{R_i} = \frac{1}{R_{Si}} + \frac{1}{R_{TaSiN}} \approx \frac{1}{R_{Si}} \tag{5.4}$$

The resistance of silicon wafer is 0.13 Ω and at least three orders of magnitude lower than the resistance of the examined conducting TaSiN thin films. As the current chooses the path with the lowest resistance, it was expected that the overall resistance stack would be determined by the silicon resistance*.

Table 5.7 *Sheet resistance for different TaSiN thin films of 100 nm thickness.*

Target Ta:Si	TaSiN	Resistance[(a)], [Ω]	Resistance[(b)], [Ω]
1:2.7	$Ta_{15}Si_{44}N_{41}$	880	800
	$Ta_{19}Si_{54}N_{26}$	170	150
	$Ta_{21}Si_{57}N_{21}$	150	57
1:1	$Ta_{22}Si_{22}N_{54}$	$35 \cdot 10^3$	$5.0 \cdot 10^3$
	$Ta_{28}Si_{28}N_{43}$	180	120
	$Ta_{33}Si_{33}N_{33}$	98	24

[(a)] Substrate Si/SiO_2 [(b)] Substrate Si

* The accuracy of the sheet resistance measurement using the four point probe is given with two significant digits and corresponds to the current source and voltmeter accuracy. In the case of the TaSiN ohmic contact to silicon, TaSiN sheet resistance can be estimated if the accuracy of the measuring apparatus has at least 5 significant digits.

Based on the results from the 4 point probe method, it was ascertained that the sheet resistance of Si/TaSiN was much higher than for the silicon and of he same order of magnitude as for bare material (Table 5.7). These findings suggest that the voltage drop across the contact is high compared with a drop across the silicon and pass no current. The p^{++}-Si/TaSiN junction develops very high contact resistance. The main current path is through the TaSiN thin layer (Figure 5.12).

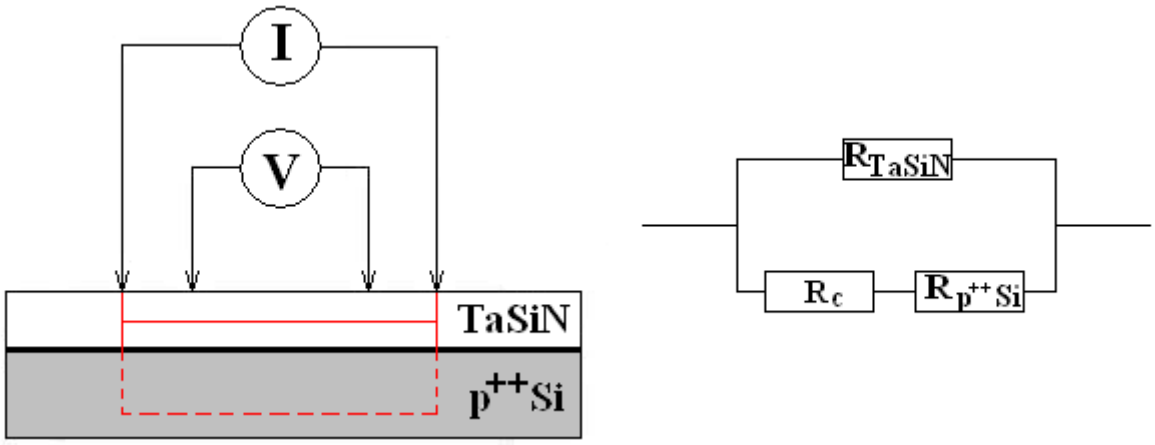


Figure 5.12 *Schematic presentation of current flow and equivalent circuit for Si/TaSiN stack (R_c-contact resistance).*

Although the silicon substrate was etched prior to TaSiN deposition, the silicone surface may have been contaminated with nitrogen and other rest gases during the flushing of vacuum chamber with sputter gas (argon and 1 % nitrogen). It is also possible that the first few monolayers of TaSiN contain more nitrogen, which leads to an interface region of TaSiN and silicon with higher resistance.

Choosing the proper material for the metallization of the p^{++}-silicon substrate can provide a low resistance ohmic contact [142-144]. In order to have an ohmic contact for holes at the metal-semiconductor interface, the work function of metal (ϕ_m) has to be larger than the work function of the semiconductor (ϕ_s), $\phi_m > \phi_s$. Contrary, for $\phi_s > \phi_m$ a Schottky-type potential barrier exists for holes at metal-semiconductor interface .

The work function for p-silicon can be calculated from the following equation [144]:

$$\Phi_{p^{++}-Si} = \chi + \frac{E_g}{q} - k_B T \cdot \ln \frac{N_v}{N_a} \qquad (5.5)$$

where χ is the electron affinity, E_g the bandgap energy ($E_g = E_c - E_v$), E_c the minimum energy of the conduction band, E_v the maximum energy of the valence band, N_v the effective density of states in the valence band and N_a the acceptor doping concentration. The silicon

energy bandgap depends on the doping concentration ($E_g = E_g(\mathrm{Si}) + \Delta Eg$) and the difference is given with empirical formula [145]:

$$\Delta E_g = -22.5 \cdot \sqrt{\frac{N_a}{10^{18}\, cm^3}} \ [\mathrm{meV}] \tag{5.6}$$

For the boron density $N_a = 10^{20}$ cm^{-3} and $E_g(\mathrm{Si}) = 1.14$ eV, the energy bandgap for p^{++}-Si is $E_g(\mathrm{p^{++}\text{-}Si}) = 0.915$ eV. The work function for p^{++}-Si substrate is $\phi(\mathrm{p^{++}\text{-}Si}) = 5.01$ eV for $N_v(\mathrm{Si}) = 1.83 \cdot 10^{19}$ cm^{-3} and $\chi(\mathrm{Si}) = 4.05$ eV [103]. The work function of platinum has the value $\phi_m = 5.3$ eV and fulfils the condition $\phi_m(\mathrm{Pt}) > \phi_s(\mathrm{p^{++}\text{-}Si})$, required for the ohmic contact for holes [89]. The energy band diagrams for a Pt/p^{++}-Si system before and after contact are presented in Figure 5.13.

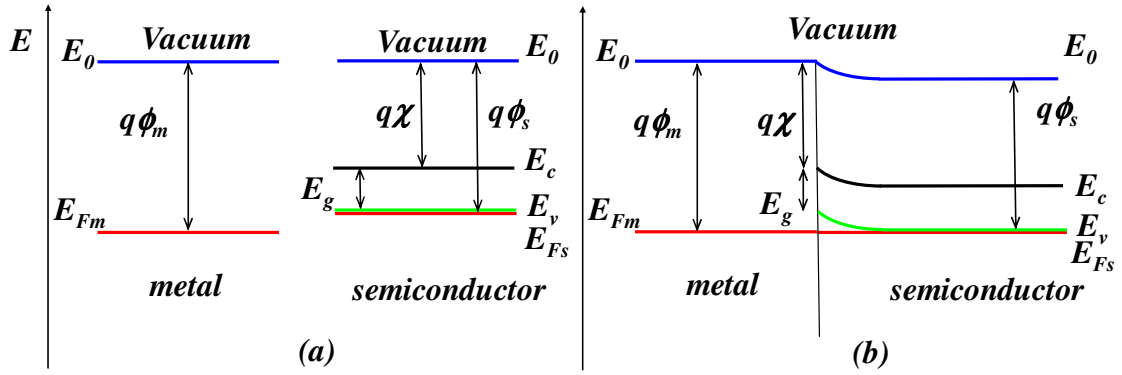


Figure 5.13 *Energy band diagram for Pt/p^{++}-silicon interface: a) before contact and b) in contact, where $E_{Fs} - E_v = -k_B T \ln(N_a / N_v) = -0.04\, eV$ (E_{Fm} and E_{Fs} are the Fermi energies for metal and semiconductor, respectively).*

Therefore, the layer sequence was changed: after etching the p^{++}-silicon substrate, the sample was closed in the vacuum chamber under base pressure $1 \cdot 10^{-7}$ mbar and a 100 nm thick platinum thin film was deposited onto the silicon by DC sputtering (Table A.2.3). The sputter gas was argon and the target power was 375 W. The sputter rate was 1.85 nm/s. Without interrupting the vacuum, TaSiN thin films were deposited onto the platinum layer using standard parameters.

Similar to the p^{++}-Si substrate an ohmic behaviour for Si/Pt and Si/Pt/TaSiN stacks was proved. The linear voltage-current dependence is presented in Figure 5.14. After deposition of the platinum layer, the slope changes slightly then remains the same after additional deposition of conductive $Ta_{21}S_{57}iN_{21}$ thin films due to the parallel connection of the layers (see Eq. 5.4 and Figure 5.15).

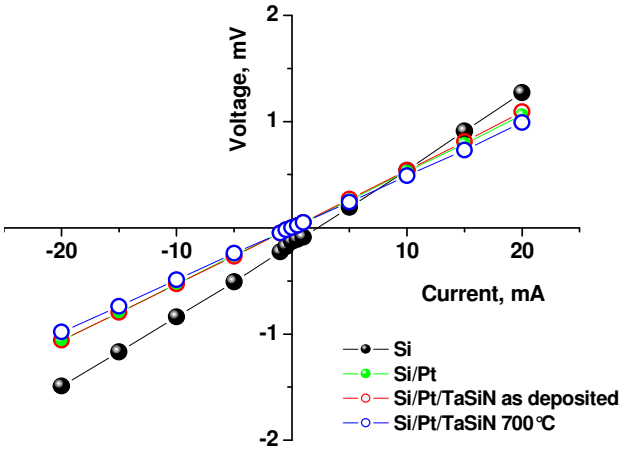


Figure 5.14 *Voltage vs. current for different stacks.*

Sheet resistance of different layers and stacks are represented in Table 5.8. The resistance of Si/Pt/TaSiN stack is the same as the silicon resistance, suggesting that the main current path is through the silicon substrate (Figure 5.15).

Table 5.8 *Sheet resistance of examined stacks.*

Sample	Sheet resistance, [Ω]
Si (etched) (substrate)	0.13
$Si/SiO_2/Pt$ (100 nm)	1.3
Si (etched)/$Ta_{21}Si_{57}N_{21}$ (100 nm)	57
Si (etched)/Pt/TaSiN	0.12

Introducing the platinum layer between silicon and the TaSiN thin film successfully reduced the contact resistance. The same ohmic behaviour was found for all of the conductive TaSiN thin films with different compositions.

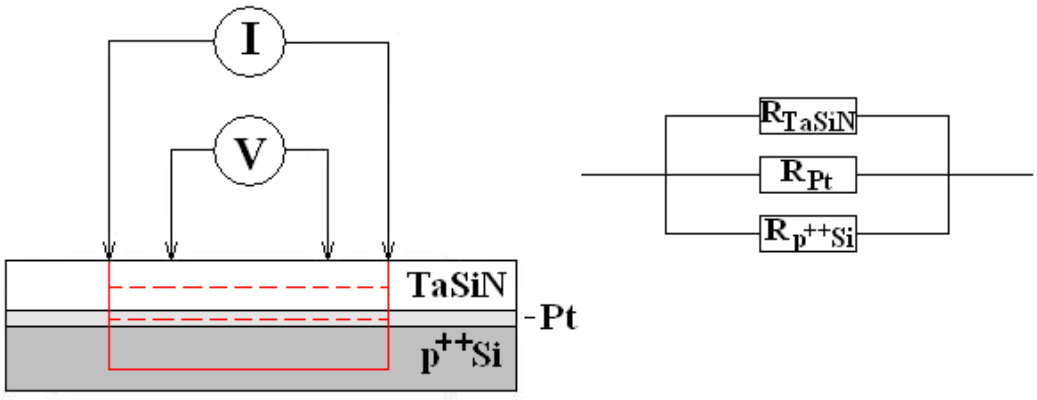


Figure 5.15 *Schematic presentation of current flow and equivalent circuit for Si/Pt/TaSiN stack.*

After deposition the Si/Pt/TaSiN stack was annealed at 500 °C, 600 °C and 700 °C in an oxygen atmosphere for 10 min in order to investigate the thermal stability of conduction through (or resistance of) the stack.

Table 5.9 *Sheet resistance and the roughness of Si/Pt/$Ta_{21}Si_{57}N_{21}$ layers as-deposited and after annealing in oxygen atmosphere.*

Treatment	Resistance, [Ω]	Roughness, [nm]
after deposition	0.12	0.39
400 °C	0.12	0.42
500 °C	0.12	0.47
600 °C	0.12	0.56
700 °C	0.12	0.67

The Si/Pt/TaSiN stack resistance does not change after annealing. When the SiO_2 insulating layer forms between the Si substrate and the Pt film, the overall resistance is determined by Pt and TaSiN resistance in parallel connection, which is ~ 1.3 Ω. The unchanged sheet resistivity of Si/Pt/TaSiN stack infers that no insulating layer between the Si and the Pt was built during annealing and that the overall resistance is still determined by silicon resistance. This proves that TaSiN thin film is sufficiently conducting and successfully serves as oxygen barrier that protects the silicon from oxidation (Table 5.9). The root mean square (*rms*) roughness changes form 0.39 nm as deposited to 0.67 nm after annealing.

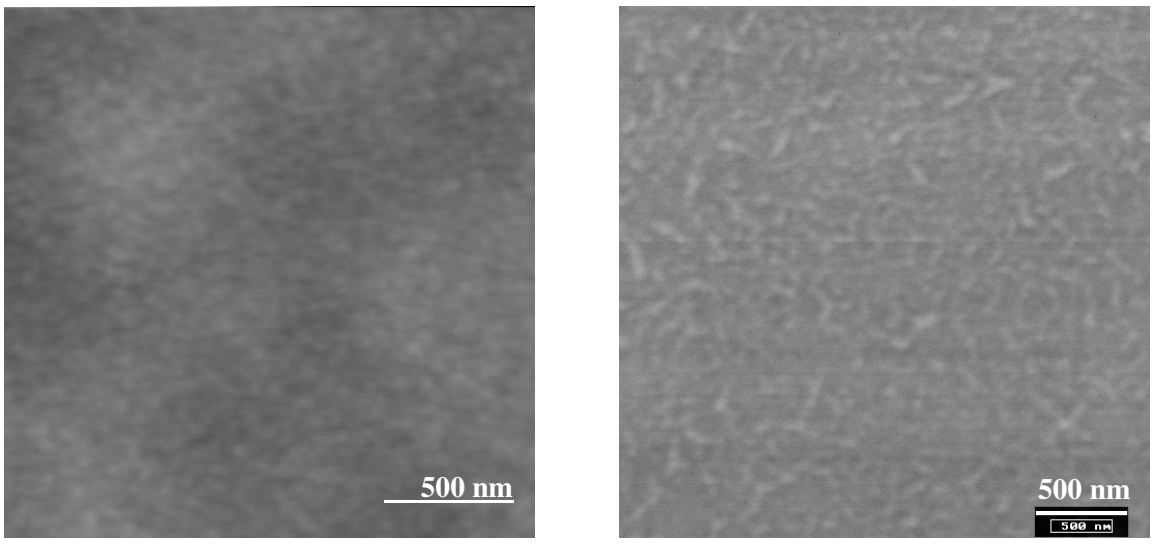


Figure 5.16 *AFM and SEM picture of $Ta_{21}Si_{57}N_{21}$ surface after RTA at 700 °C for 10 minutes in oxygen atmosphere.*

The surface morphology of uppermost TaSiN layer was observed using atomic force microscopy and scanning electron microscopy (Figure 5.16). No hillock formation is visible and the surface appears very smooth.

The XRD study of Si/Pt/TaSiN stack was performed using conventional Bragg-Brentano geometry. To accurately align the sample position with respect to the detector, the silicon (400) reflex was used in each measurement. Only platinum and silicon peaks are detected after deposition (Figure 5.17 and Table A.1.2). The platinum film is highly (111) textured, what is the usual behaviour for sputtered platinum films and for most face-centred cubic (fcc) metal films. The (111) crystal plane has the largest atomic packing density and therefore the smallest surface energy. It was expected that platinum films are under tensile stress due to big mismatch in lattice constant between silicon and platinum (a(Si) = 4.43088 Å and a(Pt) = 3.92310 Å). The platinum peak is shifted to lower 2θ values, suggesting that the film is under tensile stress [146-148].

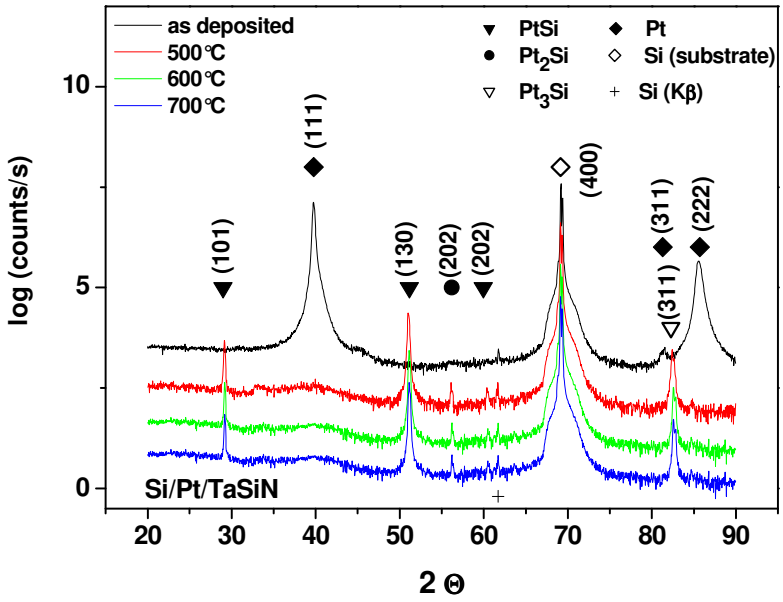


Figure 5.17 *X-Ray diagram for Si/Pt/$Ta_{21}Si_{57}N_{21}$ sample as-deposited and after annealing at 500 °C, 600 °C und 700 °C in an oxygen atmosphere.*

New different platinum silicide phases, orthorhombic PtSi, tetragonal Pt_2Si and cubic Pt_3Si, are observed in diffraction spectra in Figure 5.17 for Si/Pt/TaSiN stack after annealing at different temperatures. The identified peaks of various silicide phases are listed in Table A.1.2. The most pronounced peaks come from PtSi phase, with (101) and (130) as preferred orientations. The weak peaks show the presence of Pt_2Si phase at elevated temperatures. The cubic Pt_3Si phase is present with (311) as preferred orientation. As the platinum peaks are disappeared after annealing at temperatures above 500 °C a complete silicidation of the Pt

film is observed. The platinum silicide layer is under compressive stress after annealing concluded from the peak shift.

It has been reported previously that the PtSi phase growth proceeds via complete conversion of Pt to Pt_2Si followed by complete conversion to a single phase PtSi at higher temperatures [149]. The low resistivity polycrystalline platinum silicides ($\rho(Pt_xSi) = 3.2 \cdot 10^{-7}\ \Omega m$) are formed at the temperatures above 323 °C [41, 150, 151].

In order to analyse the reaction between platinum and silicon substrate, 100 nm thick platinum layer was deposited on silicon substrate and exposed to the same thermal treatment as Si/Pt/TaSiN sample. The X ray diffraction spectra in Figure 5.18 show the same platinum silicide phases and corresponding preferred orientations as for the Si/Pt/TaSiN sample (Table A.1.3). The platinum peak is still visible after annealing, although the intensity decreases due to reaction with silicon. The (311) Pt reflex disappeared totally, presumed through the reaction with silicon, forming the (311) cubic Pt_3Si phase.

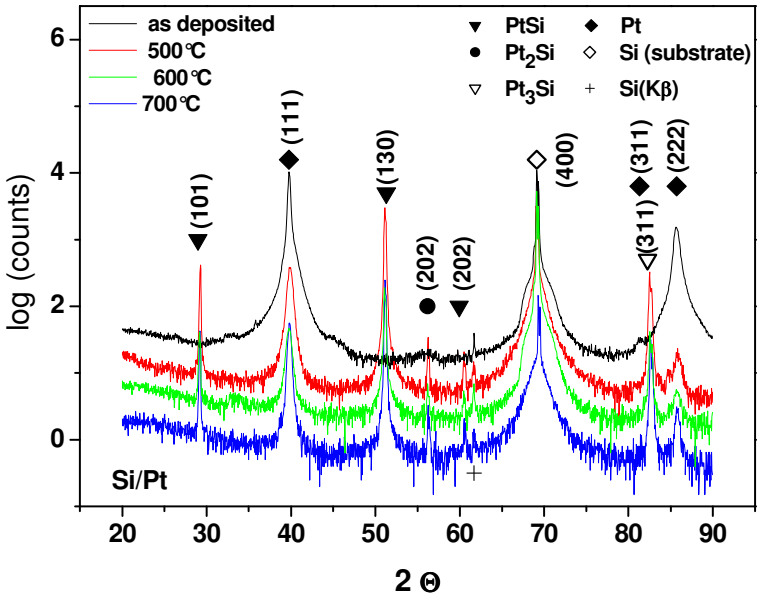


Figure 5.18 *X-Ray diagram for Si/Pt sample as-deposited and after annealing at 500 °C, 600 °C und 700 °C in an oxygen atmosphere.*

It is a well documented that platinum films on a silicon single crystal substrate are completely transformed into PtSi when annealed above 500 °C in an inert atmosphere such as nitrogen [40, 149, 152]. But in an oxygen atmosphere the reaction stopped about 500 Å below the surface. The oxygen permeates the platinum layer and reacts with silicon forming SiO_2 at the interface PtSi to Pt. The formation of SiO_2 blocks the diffusion paths for silicon and platinum and inhibits further reaction. The absence of the platinum (111) peak in the XRD pattern following annealing above 500 °C indicates that the complete silicidation of the platinum

underlayer in Si/Pt/TaSiN stack occurred and that no oxygen diffusion through the TaSiN took a place. The TaSiN layer has a good barrier effect for oxygen diffusion.

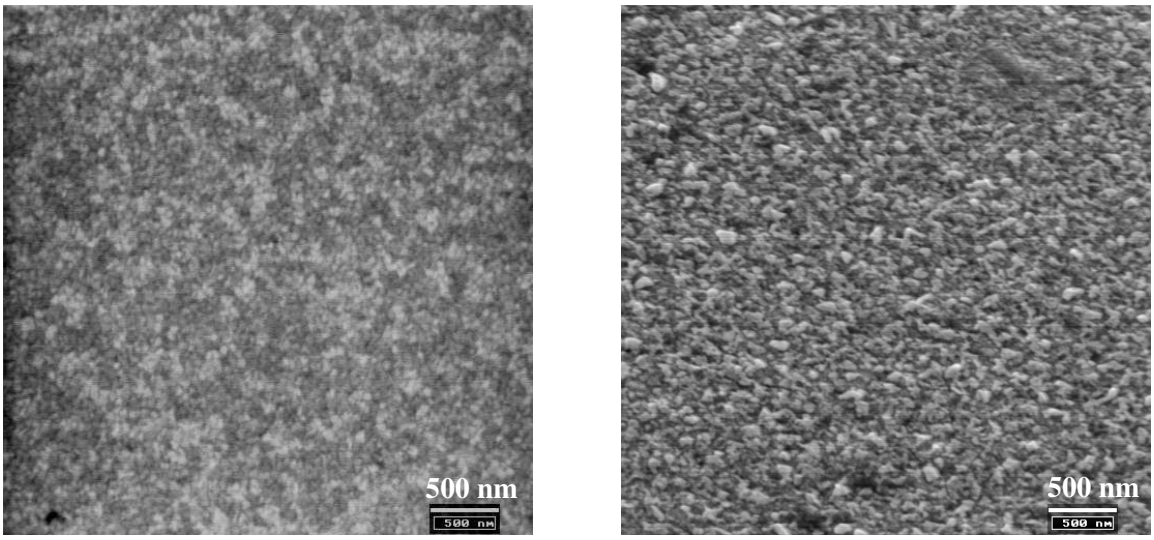


Figure 5.19 *SEM picture of platinum layer in Si/Pt stack before and after annealing at 700 °C in oxygen for 10 minutes.*

After deposition, the platinum thin films are dense after deposition with fine grain structure (Figure 5.19). The root mean square (*rms*) roughness is 0.503 nm. After annealing, the surface appears very rough as a result of platinum silicide formation. The sheet resistance after annealing does not change and is determined with silicon resistance (Table 5.10).

Table 5.10 *Sheet resistance and the roughness of Si/Pt stack as-deposited and after annealing in oxygen atmosphere.*

Treatment	Resistance, [Ω]	Roughness, [nm]
after deposition	0.12	0.50
500 °C	0.12	13.00
600 °C	0.12	11.86
700 °C	0.12	12.10

5.2 Properties of thin film stack

5.2.1 Si/Pt/TaSiN/Pt

Because the deposition of $BaTiO_3$ directly on TaSiN results in lowering the overall capacitance an additional layer was introduced between dielectric material and TaSiN layer Because of its high conductivity and its high Schottky barrier height on BTO or BST dielectrics, platinum was considered to be a suitable material. These properties give rise to a low leakage current in a capacitor system with high κ-materials (titanates). Platinum layers with 100 nm and 200 nm thickness were deposited on the TaSiN thin films using standard sputter parameters (Table A.2.3). The deposition temperatures were at room temperature (RT) and 400 °C. It is important to mention, that the sputter system Leybold Univex 450B has the possibility to deposit multi-layered system without breaking the vacuum. All samples were made without interrupting the vacuum, in order to avoid exposure to the air and the contamination of the interface with oxygen.
The stacks were characterised in terms of roughness, morphology and sheet resistance after deposition and after annealing at temperatures between 500 °C and 700 °C (Table 5.11).

Table 5.11 *Sheet resistance and the roughness of different Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt stacks before and after annealing in oxygen atmosphere.*

Pt thickness/ deposition t, [°C]	Characterization	as-deposited	500 °C	600 °C	700 °C
100 nm/RT	Roughness, [nm]	1.99	11.93	10.24	12.74
	Resistance, [Ω]	0.11	0.20	0.20	0.80
200 nm/RT	Roughness, [nm]	1.59	17.99	13.28	17.38
	Resistance, [Ω]	0.10	0.18	0.18	0.19
100 nm/400 °C	Roughness, [nm]	2.02	17.70	15.60	10.81
	Resistance, [Ω]	0.11	0.18	0.18	0.80

The 100 nm thick platinum layer deposited at room temperature has a fine grain structure with *rms* roughness of 2.0 nm. The overall resistance was determined with the silicon resistance and has Ohmic behaviour, as expected. The contact resistance between as-deposited platinum layer and TaSiN has no influence on voltage drop in the stack. After annealing of the Si/Pt/TaSiN/Pt sample, the platinum surface becomes very rough and the overall resistance

increases (Figure 5.20). After the treatment at 700 °C many holes were observed, probably due to the increase of tensile stress and volume shrinkage [38, 39, 44-47, 153-155].

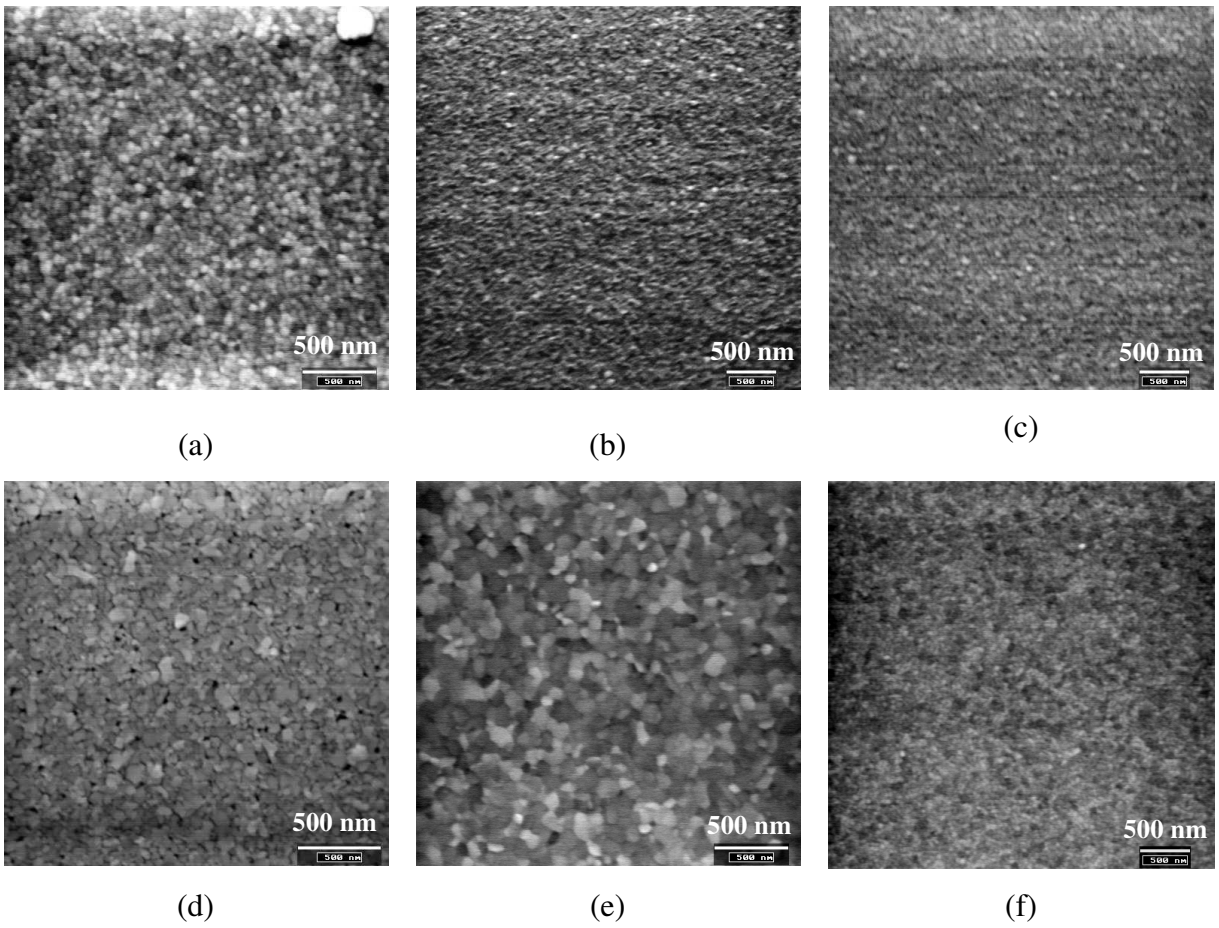


Figure 5.20 *SEM image of platinum upper layer in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt(100 nm, RT) stack for several annealing temperatures: a) as-deposited b) 500 °C c) 600 °C d) 700 °C e) as-deposited Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt(200 nm, RT) and f) Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt(100 nm, 400 °C).*

The platinum thin layers are strongly (111) textured and under compressive stress when deposited on amorphous TaSiN layer (Figure 5.21 and Table A.1.4). Small (311) and (200) platinum peaks were found and 2θ shift to smaller values, due to tensile strain. Polycrystalline thin films on substrates are often in a state of biaxial strain [156]. The stress and grain energy density vary from grain to grain, depending on the crystallographic orientations or textures. PtSi and Pt_2Si phase were found after deposition of the upper platinum layer. It is assumed that, in the beginning of the sputter deposition platinum atoms react with the TaSiN surface forming polycrystalline Pt_xSi. Such a reaction leads to improved adhesion and reduced contact resistance of the platinum layer to TaSiN. After annealing the Si/Pt/TaSiN/Pt sample new Pt_xSi phases were found and compared to the XRD pattern of Si/Pt/TaSiN stack. This

finding suggests that the upper platinum layer reacts with TaSiN layer forming polycrystalline Pt_xSi. The reaction already takes place at 400 °C (R_S = 0.14 Ω, *rms* = 4.05 nm) [41].

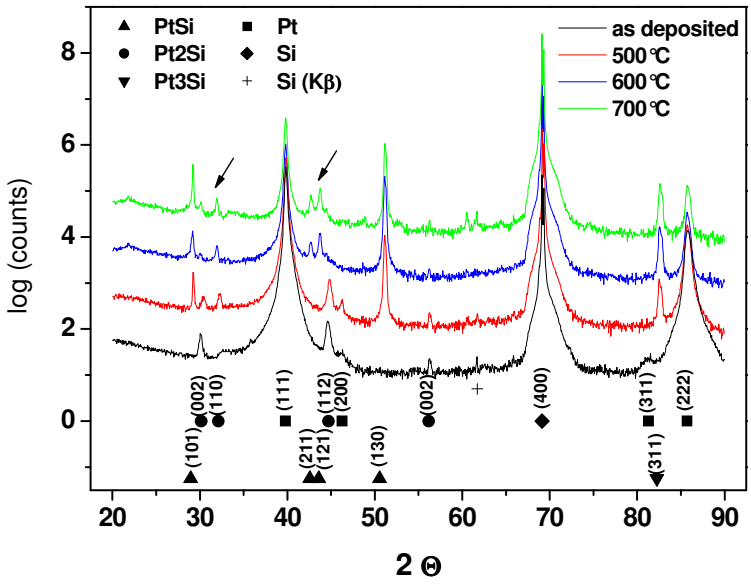


Figure 5.21 *X-ray diagram for Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt sample as-deposited and after annealing at 500 °C, 600 °C and 700 °C in oxygen atmosphere.*

After annealing, the intensity of platinum peaks is lower, suggesting the conversion of platinum to platinum silicide. A thicker platinum layer (200 nm) could not delay the oxidation of silicide layer. Furthermore, the resistance measurement shows the same behaviour like for the 100 nm thick platinum upper layer. The grain size of the platinum layer increases with thickness. Increasing the deposition temperature (400 °C) of platinum layer does not improve the behaviour.

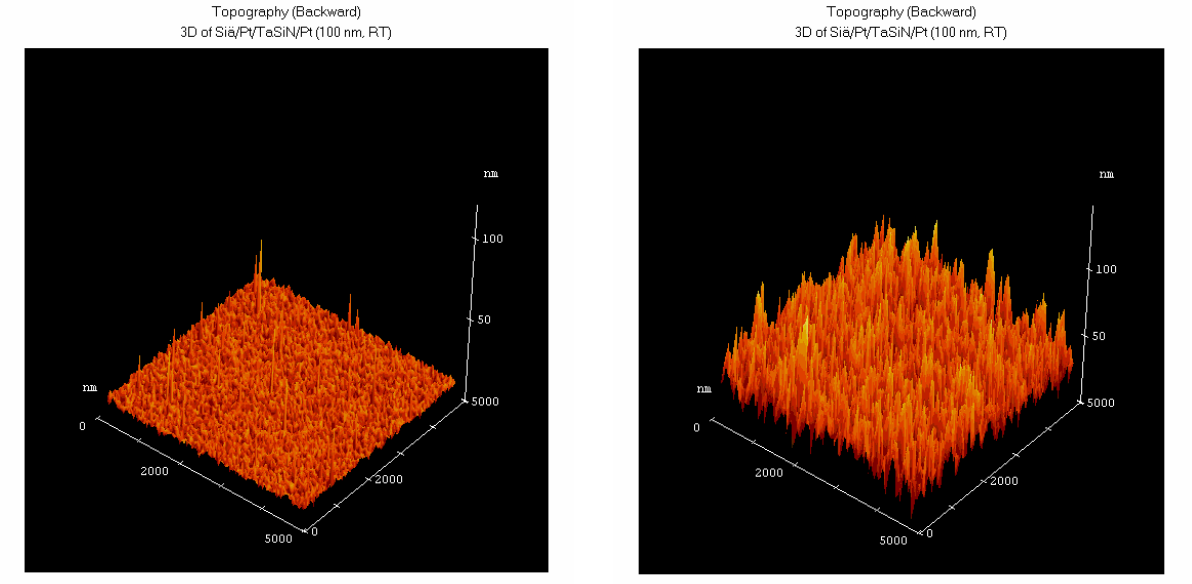


Figure 5.22 *AFM picture of platinum top layer in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt (RT, 100 nm) stack as-deposited and after annealing at 700 °C.*

The resistance and roughness of upper platinum layer increase dramatically (Figure 5.22). Probably, oxygen diffuses through the platinum grain boundaries and reacts with silicide forming SiO_2.

The cross section of Si/Pt/TaSiN/Pt after annealing in oxygen atmosphere at 700 °C shows that the platinum layer on silicon is totally consumed and transformed in Pt_xSi (Figure 5.23). The change in the TaSiN colour is presumable due to platinum diffusion and silicide formation. The upper platinum layer is irregularly distributed.

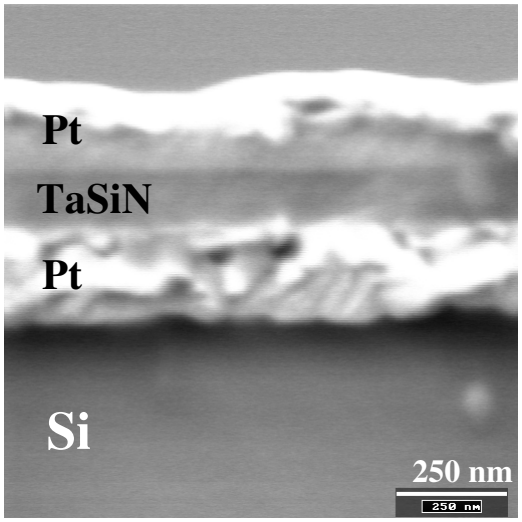


Figure 5.23 *SEM picture of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt stack's cross section.*

The reaction of the upper platinum layer with TaSiN can be seen from RBS spectra, too (Figure 5.24). Pt_xSi layer was formed after annealing at 500 °C. Simultaneously, the lower platinum layer reacts with silicon substrate and the upper TaSiN layer, being totally consumed and converted into Pt_xSi. The Pt_xSi from the upper layer intermixes with TaSiN at temperatures above 600 °C. Since the silicide layer is too thick, resulting in the silicon signal overlapping the oxygen signal, the oxygen could not be properly detected.

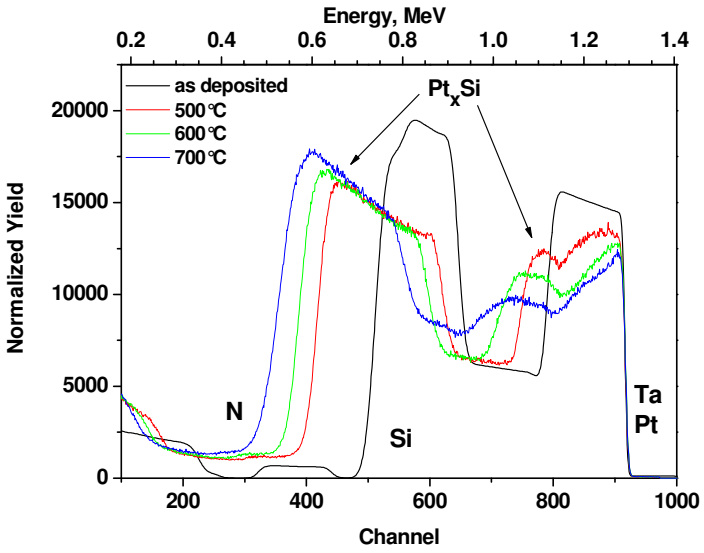


Figure 5.24 *RBS spectra for Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt stack as-deposited and after annealing at different temperatures.*

These results indicate that platinum readily reacts with $Ta_{21}Si_{57}N_{21}$ to form silicide [132]. This reaction is presumably due to the high concentration of silicon in the TaSiN layer. Further TaSiN compositions were investigated in Si/Pt/TaSiN/Pt stacks. Only $Ta_{22}Si_{22}N_{54}$ was excluded from further investigation, due to its very high resistivity as well as its insulating behaviour after annealing in oxygen atmosphere. Sheet resistance and *rms* roughness are listed in Table 5.12 and schematically depicted in Figure 5.25 and Figure 5.26.

Similar behaviour was found for the samples that had TaSiN with a ratio of Ta to Si of approximately 2.8. The sheet resistance of Si/Pt/$Ta_{15}Si_{44}N_{41}$/Pt stack after deposition has the value of 100 nm thick platinum layer, suggesting that the $Ta_{15}Si_{44}N_{41}$/Pt junction develops very high contact resistance. No change in the resistance was found after annealing; however a roughening of the surface occurred, presumably due to adhesion problems of platinum on the oxide thin film. For the $Ta_{19}Si_{54}N_{26}$ stack, the overall sheet resistance after deposition was determined by the silicon substrate; however the value increased after annealing and then remained constant.

Table 5.12 *Sheet resistance and the roughness (rms) of Si/Pt/TaSiN/Pt layers for different TaSiN compositions as-deposited and after annealing in oxygen atmosphere.*

Stack	**Si/Pt/$Ta_{28}Si_{28}N_{43}$/Pt**	
Treatment	Rs, [Ω]	rms, [nm]
after deposition	0.13	1.40
500 °C	0.13	1.70
600 °C	0.13	2.50
700 °C	0.13	5.86
Stack	**Si/Pt/$Ta_{33}Si_{33}N_{33}$/Pt**	
after deposition	0.13	5.50
500 °C	0.13	9.21
600 °C	0.13	5.24
700 °C	0.13	6.19
Stack	**Si/Pt/$Ta_{15}Si_{44}N_{41}$/Pt**	
after deposition	1.2	2.79
500 °C	1.2	5.69
600 °C	1.2	4.92
700 °C	1.2	7.90
Stack	**Si/Pt/$Ta_{19}Si_{54}N_{26}$/Pt**	
after deposition	0.13	1.05
500 °C	2.1	5.02
600 °C	2.1	4.83
700 °C	2.1	6.78

The Si/Pt/TaSiN/Pt stacks with Ta to Si ratio 1 showed different behaviour, presumably due to the lower reactivity of TaSiN to platinum due to the lower silicon content. The sheet resistance remained constant, even after annealing, although the surface became rough. Specifically, the sample with $Ta_{33}Si_{33}N_{33}$ was rough even after deposition. In addition, an adhesion problem was observed between the platinum and TaSiN surfaces.

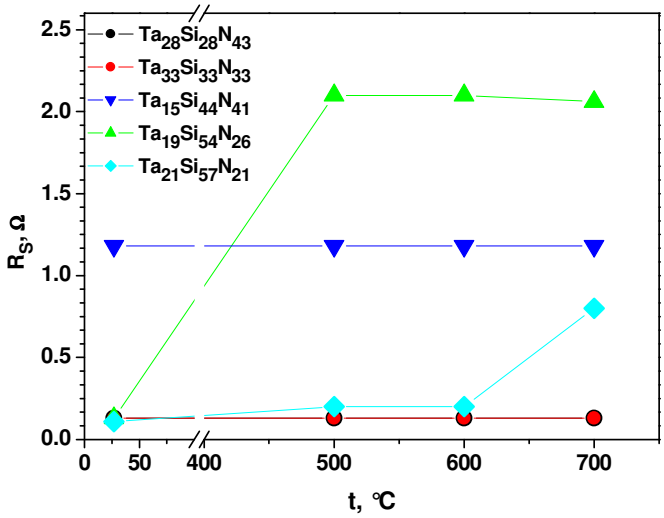


Figure 5.25 *Sheet resistance dependence on temperature for Si/Pt/TaSiN/Pt stack for different TaSiN compositions.*

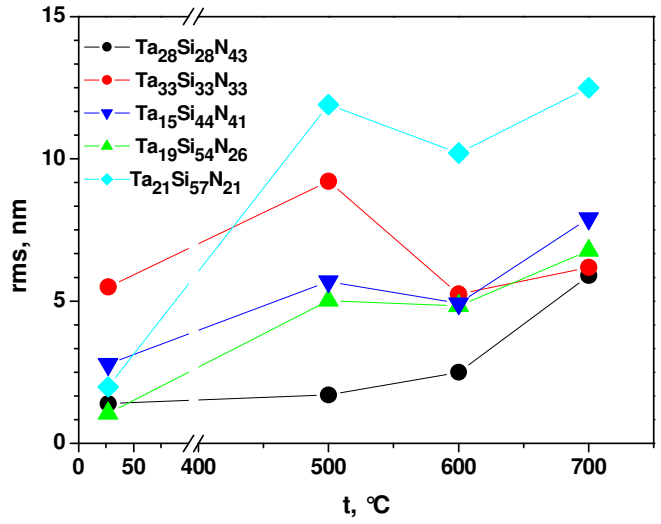


Figure 5.26 *Roughness dependence on temperature for Si/Pt/TaSiN/Pt stack for different TaSiN compositions.*

Based on the XRD spectra no new crystal phase was detected; however, the RBS measurements showed some changes at the TaSiN/Pt interface (Figure 5.27, Figure 5.28 and Table A.1.5). While the top platinum layer remained unreacted, a reaction or intermixing with silicon was detected at the interface. However, no crystal phase was formed.

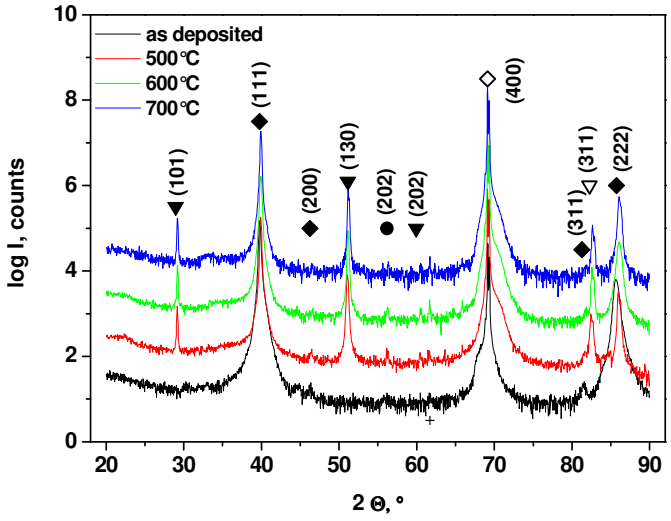


Figure 5.27 *XRD pattern for Si/Pt/$Ta_{33}Si_{33}N_{33}$/Pt stack as-deposited and after annealing in oxygen atmosphere.*

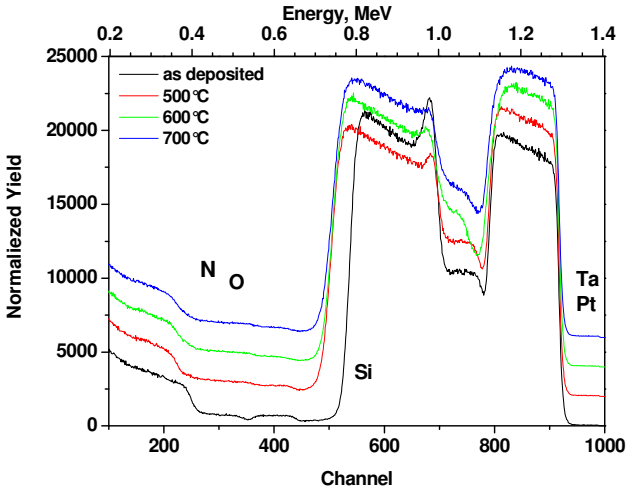


Figure 5.28 *RBS spectra for Si/Pt/$Ta_{33}Si_{33}N_{33}$/Pt stack as-deposited and after annealing in oxygen atmosphere.*

The behaviour of Si/Pt/$Ta_{28}Si_{28}N_{43}$/Pt is very interesting especially since the $Ta_{28}Si_{28}N_{43}$ film without the Pt top layer was not conductive after annealing in the same condition (Table A.1.6). It is difficult to believe that the platinum protects TaSiN from oxidation due to the fact that platinum is very permeable to oxygen.

5.2.2 Si/Pt/TaSiN/Ta/Pt

Since the platinum reacted with the TaSiN layer at higher silicon content, a 4 nm thick tantalum barrier layer was placed between TaSiN and upper platinum thin film. A 100 nm thick platinum film was subsequently deposited at room temperature (Table A.2.4). Although

the sheet resistance of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ta/Pt stack presented no alteration after the annealing process, the roughness changed drastically (Table 5.13).

Table 5.13 *Sheet resistance and roughness of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ta/Pt stack as-deposited and after annealing at different temperatures in oxygen atmosphere.*

Treatment	Sheet resistance, [Ω]	Roughness, [nm]
as-deposited	0.15	0.99
500 °C	0.15	7.03
600 °C	0.15	10.90
700 °C	0.16	43.38

Especially after annealing at 700 °C, a rough granular layer completely covered the surface. Loss of adhesion is seen in the spherical, delaminated regions (Figure 5.29). The surface is not suitable for the deposition of a thin dielectric film.

Similar to the Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt sample, no Pt_xSi crystalline phase was observed after deposition of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ta/Pt stack (Figure 5.30). As such, it is reasonable to state that the tantalum barrier successfully prohibits the interaction between the platinum atoms and the TaSiN layer, which may occur at the beginning of the sputter process. Interestingly, following the annealing process, the XRD patterns of these two samples are almost identical (Table A.1.7). Nevertheless, some differences were observed in the RBS spectra (Figure 5.31). The unreacted platinum layer was left on the surface and the intermixing of Pt_xSi phase and TaSiN was not as intensive as in the Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt sample.

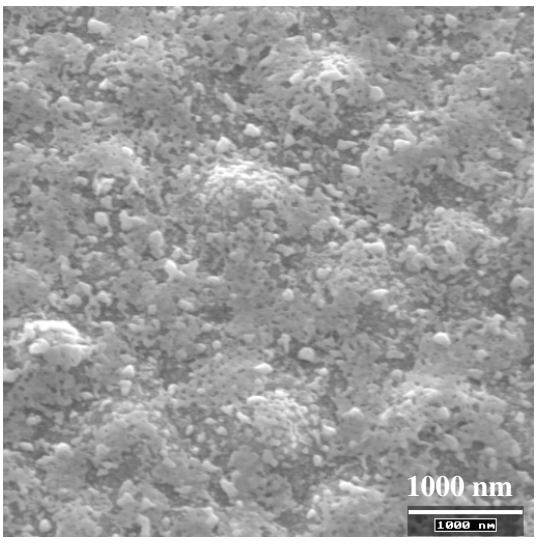


Figure 5.29 *SEM picture of to platinum layer in Si/Pt/TaSiN/Ta/Pt stack after annealing at 700 °C in an oxygen atmosphere.*

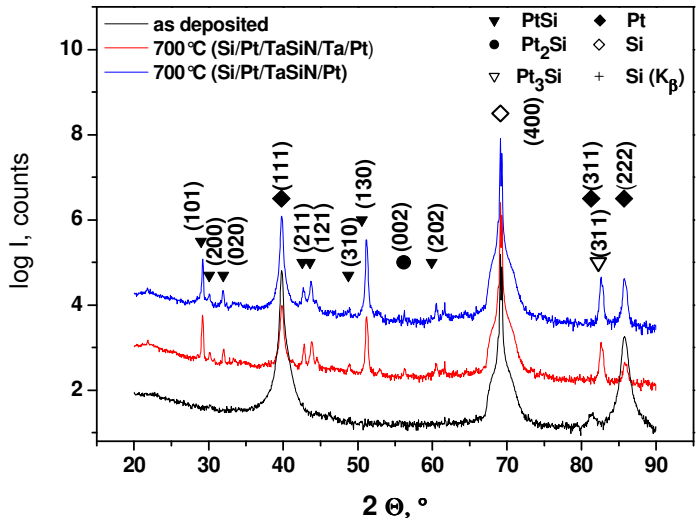


Figure 5.30 *X-ray diagrams for Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ta/Pt sample as-deposited and after annealing at 700 °C in an oxygen atmosphere (comparison with Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt stack).*

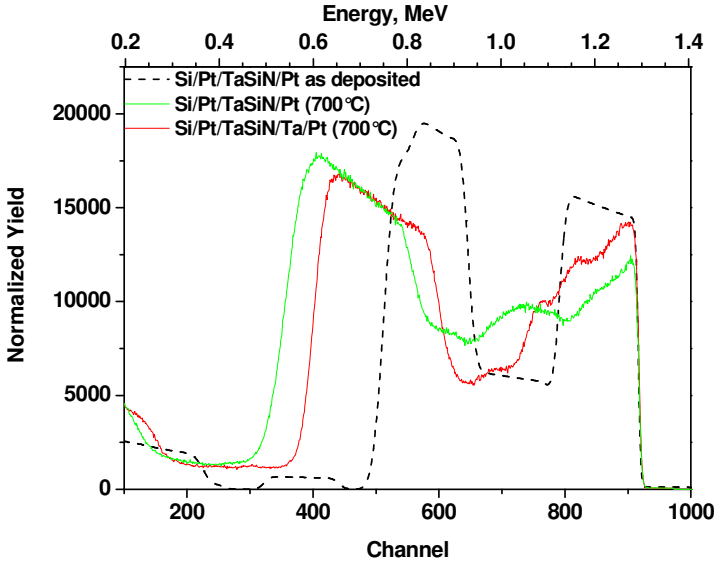


Figure 5.31 *RBS spectra for Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ta/Pt and Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt samples after annealing in an oxygen atmosphere for 10 min at 700 °C*

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5.2.3 Si/Pt/TaSiN/Ir

The reactivity of TaSiN thin films as barrier material with the top platinum layer has a negative influence on thermal stability for the proposed Si/Pt/TaSiN/Pt stack. The surface roughening and/or increase of overall resistance render them unsuitable for applications as bottom electrodes in the p^{++}-Si/ electrode stack/ dielectric material system. Further investigations include the other noble metal, iridium (Ir), a material with thermal stability, low resistivity and high work function.

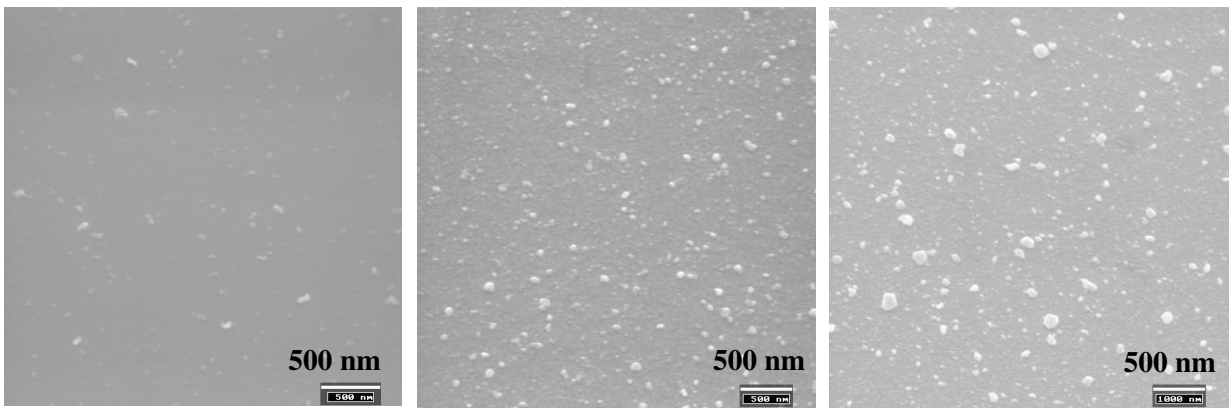
The 100 nm thick iridium thin film was deposited *ex-situ* in a DC magnetron sputter system. After deposition of the Si/Pt/TaSiN stack, the iridium layer was sputtered following a one day air exposure. The sputter parameters are listed in Table A.2.5. The deposited iridium thin film is very smooth (*rms* = 0.54 nm), but the surface roughness after annealing at 600 °C and

especially at 700 °C is even more pronounced than for the platinum films as shown in Table 5.14.

Table 5.14 *Sheet resistance and roughness of top iridium layer in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir stack as-deposited and after annealing in oxygen atmosphere at different temperatures.*

Treatment	Sheet resistance, [Ω]	Roughness, [nm]
as-deposited	0.15	0.54
500 °C	0.15	0.95
550 °C	0.15	0.70
600 °C	1.72	9.58
700 °C	1.35	25.59

The hillock formation at 500 °C is usually contributed to relaxation of compressive stress after room temperature deposition (Figure 5.32) [157]. The sheet resistance of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir stack remains constant after annealing at temperatures below 600 °C. Higher annealing temperatures cause an increase in surface roughening and sheet resistance increase.



(a) (b) (c)

Figure 5.32 *SEM picture of top iridium layer in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir stack after annealing at a) 550 °C b) 600 °C d) 700 °C in oxygen atmosphere.*

No iridium peak was found in the XRD diagram of the as-deposited films, suggesting that when deposited at room temperature iridium has a fine nanocrystalline structure [158].

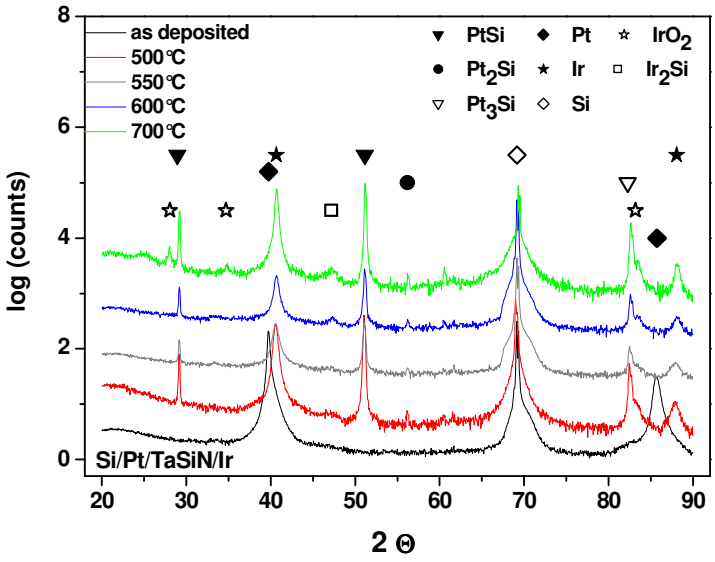


Figure 5.33 *X-ray diagram of the $Si/Pt/Ta_{21}Si_{57}N_{21}/Ir$ sample as-deposited and after annealing at 500 °C, 600 °C and 700 °C in an oxygen atmosphere.*

Detailed evaluation of the XRD diagram shows new crystal phases after annealing at 600 °C, IrO_2 and Ir_2Si (Figure 5.33 and Table A.1.8). It has been reported that – when heated in oxygen – the iridium surface oxidation occurs, forming IrO_2, rather than oxygen absorption [40]. The first silicide phase for Ir on a silicon substrate is IrSi at temperatures as low as 400 °C. Further reactions at temperatures between 400 °C and 550 °C produce $IrSi_{1.75}$. However, when heated on $Ta_{21}Si_{57}N_{21}$ the first silicide form is Ir_2Si. Iridium-oxide is conductive ($\rho \approx 3 \cdot 10^{-7}$ Ωm). In fact, both IrSi and Ir_2Si are conductive. Conversely, $IrSi_{1.75}$ has semi-conductive properties ($\rho \approx 1 - 5 \cdot 10^{-2}$ Ωm). Since only the Ir_2Si phase was found, the formation of silicide phase is expected to have no influence on the overall resistance.

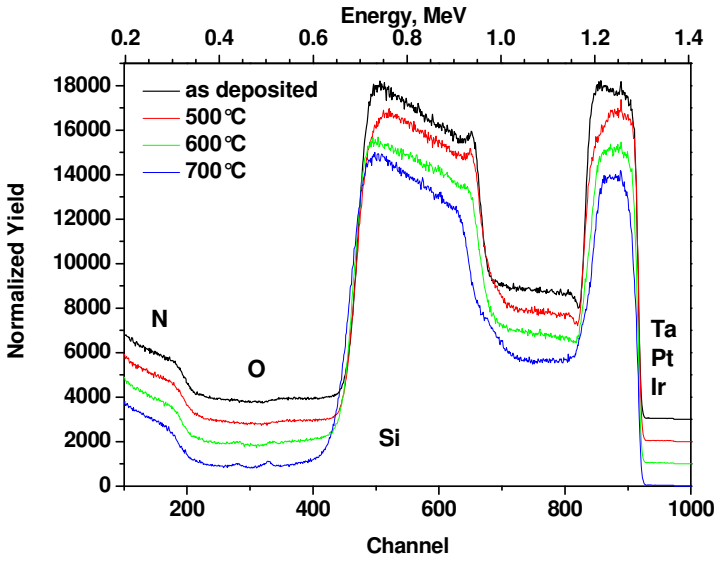


Figure 5.34 *RBS spectra for the $Si/Pt/Ta_{21}Si_{57}N_{21}/Ir$ stack after deposition and after annealing at different temperatures in an oxygen environment.*

The RBS analysis identified the oxide layer (after annealing at 600 °C and 700 °C) at the surface as IrO_2 (Figure 5.34). Conversely, in the RBS spectra, another oxygen signal was found at the interface between iridium and TaSiN layer, which may lead to an increase in the overall resistance. The new oxide phase was not detected by XRD, presumably due to its lack of crystal structure and thus amorphous state. Most likely, SiO_2 formed.

Although iridium reacts with $Ta_{21}Si_{57}N_{21}$ and forms silicide, a significant reaction rate for iridium occurs only at a considerably higher temperature (600 °C) than for platinum (400 °C). The reactivity of iridium to silicon is not as pronounced as in the case of platinum. In addition, the other TaSiN compositions, which were defined in the beginning of this research, were investigated in Si/Pt/TaSiN/Ir stacks in terms of thermal stability. The criteria for the study included sheet resistance, roughness and morphology (Table 5.15). $Ta_{22}Si_{22}N_{54}$ was excluded from investigation due its high resistivity and insulating behaviour after thermal treatment.

The stacks with TaSiN thin films with Ta to Si ratio of 1 do not demonstrate any changes in resistance after annealing at elevated temperatures. The resistance of individual thin films (iridium and platinum on insulating Si/SiO_2 substrate) decreases about 10 % after annealing, due to the relaxation processes in the material after heating, thereby lowering the overall resistance of the stacks. The surface roughness is extremely high after annealing at 700 °C, making it impossible to use such stacks as bottom electrode for dielectric film (Figure 5.35).

Table 5.15 *Sheet resistance and the roughness of top iridium thin film in Si/Pt/TaSiN/Ir stack for different TaSiN compositions (as-deposited and after annealing in oxygen atmosphere).*

Stack	**Si/Pt/$Ta_{28}Si_{28}N_{43}$/Ir**	
Treatment	Resistance, [Ω]	Roughness, [nm]
after deposition	0.16	0.71
500 °C	0.14	2.46
600 °C	0.14	4.07
700 °C	0.14	35.04
Stack	**Si/Pt/$Ta_{33}Si_{33}N_{33}$/Ir**	
after deposition	0.16	0.46
500 °C	0.14	3.03
600 °C	0.14	7.55
700 °C	0.14	47.69
Stack	**Si/Pt/$Ta_{19}Si_{54}N_{26}$/Ir**	
after deposition	0.13	1.54
500 °C	0.13	4.93
600 °C	0.53	11.84
700 °C	0.88	50.35
Stack	**Si/Pt/$Ta_{15}Si_{44}N_{41}$/Ir**	
after deposition	1.7	3.16
500 °C	1.7	3.95
600 °C	1.6	9.35
700 °C	1.6	39.34

The stacks with TaSiN/Ir thin films with Ta to Si ratio of 2.9 have a similar characteristic as the samples with Pt top electrode. The resistance of Si/Pt/$Ta_{19}Si_{54}N_{26}$/Ir stack increases after thermal treatment. The sheet resistance of Si/Pt/$Ta_{15}Si_{44}N_{41}$/Ir stack has a resistance greater than that of pure iridium. No explanation could be formulated for this behaviour. Furthermore, no resistance change was found after annealing. And, the surface roughness reaches extreme values after annealing at 700 °C, probably due to adhesion problems.

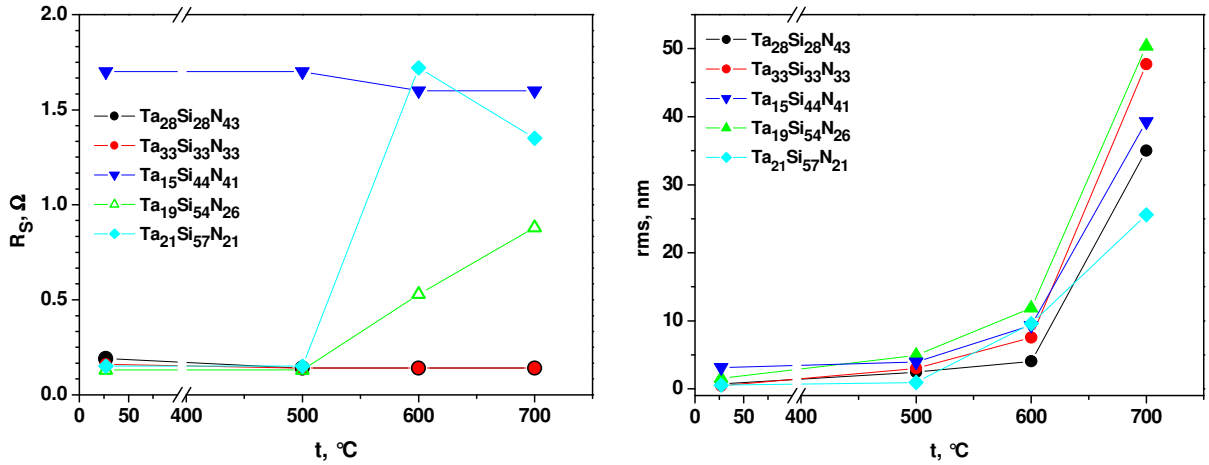


Figure 5.35 *Sheet resistance and surface roughness for Si/Pt/TaSiN/Ir stack with different TaSiN compositions at elevated temperatures.*

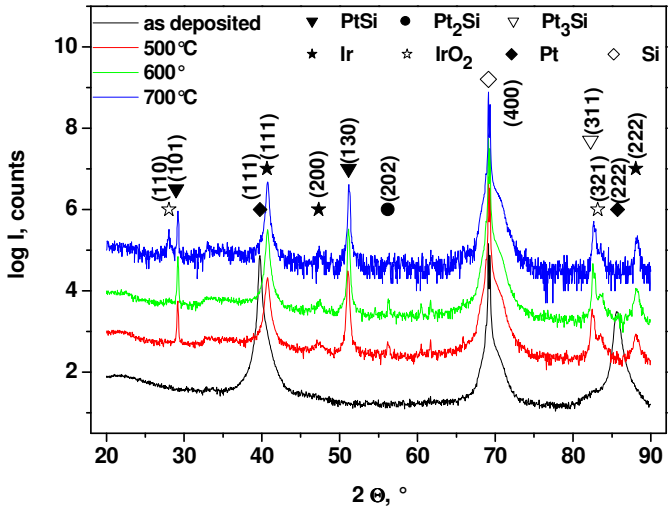


Figure 5.36 *XRD pattern for the Si/Pt/$Ta_{33}Si_{33}N_{33}$/Ir stack after deposition and after annealing in an oxygen atmosphere.*

The formation of IrO_2 with (110) and (321) texture after annealing at 600 °C in an oxygen environment was found in the x-ray diffractogram (Figure 5.36). No iridium silicide phase was detected. The RBS analysis confirmed the oxidation of the iridium surface in the Si/Pt/$Ta_{33}Si_{33}N_{33}$/Ir sample (Figure 5.37). It seems that no reaction occurred at the interface between the $Ta_{33}Si_{33}N_{33}$ thin film and the iridium layer.

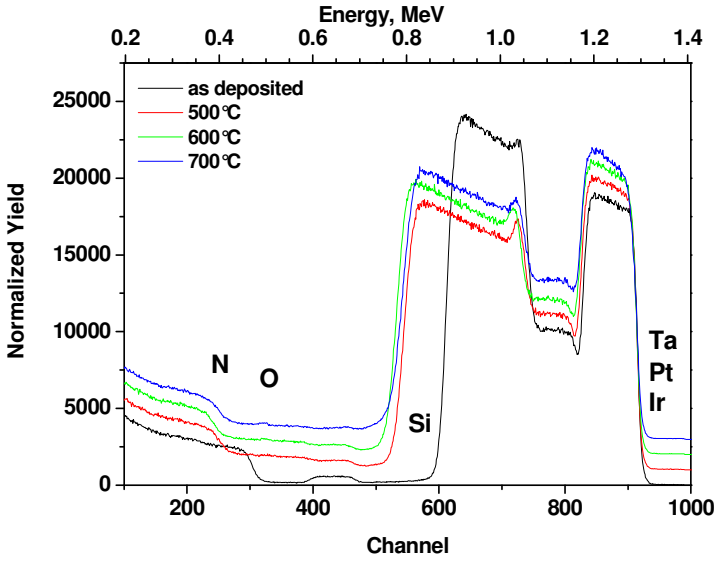


Figure 5.37 *RBS spectra for the Si/Pt/$Ta_{33}Si_{33}N_{33}$/Ir stack after deposition and after annealing in an oxygen atmosphere.*

5.3 Structure and morphology of thin dielectric films

This section focuses on a brief description of the experimental procedure for the fabrication of the thin dielectric films using diverse stacks and is followed by the characterisation in the as-deposited state.

5.3.1 Si/Pt/TaSiN/BTO

The results have shown that $Ta_{21}Si_{57}N_{21}$ remains conductive and amorphous after annealing in an oxygen atmosphere. These properties make it suitable for application as bottom electrode in capacitor system Si/Pt/TaSiN/(BTO or BST).

The dielectric $BaTiO_3$ (BTO) thin films were deposited by chemical solution deposition using a 0.1 M $BaTiO_3$ solution. The preparation procedure is shown in Figure 5.38. $BaTiO_3$ solution was prepared from barium propionate and titanium n-butoxide stabilized in acetyl acetone. At first, the barium propionate was derived by dissolving $BaCO_3$ in propionic acid. The second, acetyl acetone was added to a solution of titanium butoxide in butanol. After chelation was completed, indicated by the solution taking on a dark yellow colour, this solution was added to the propionate solution.

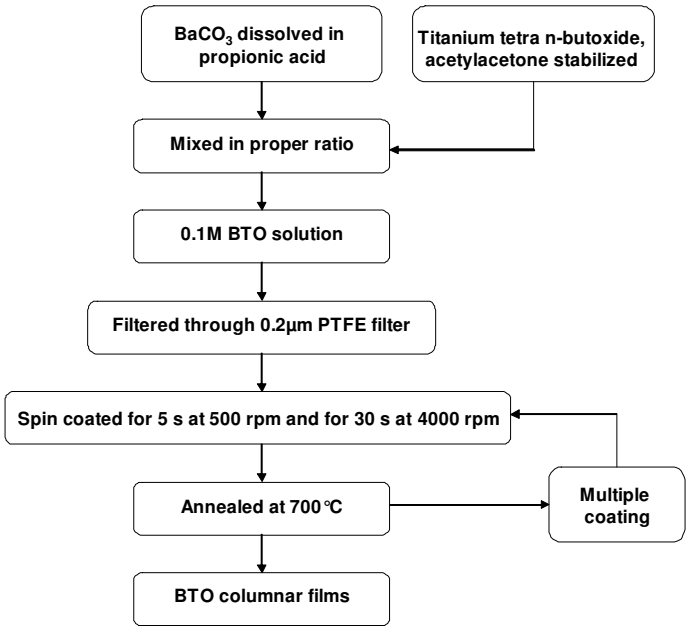
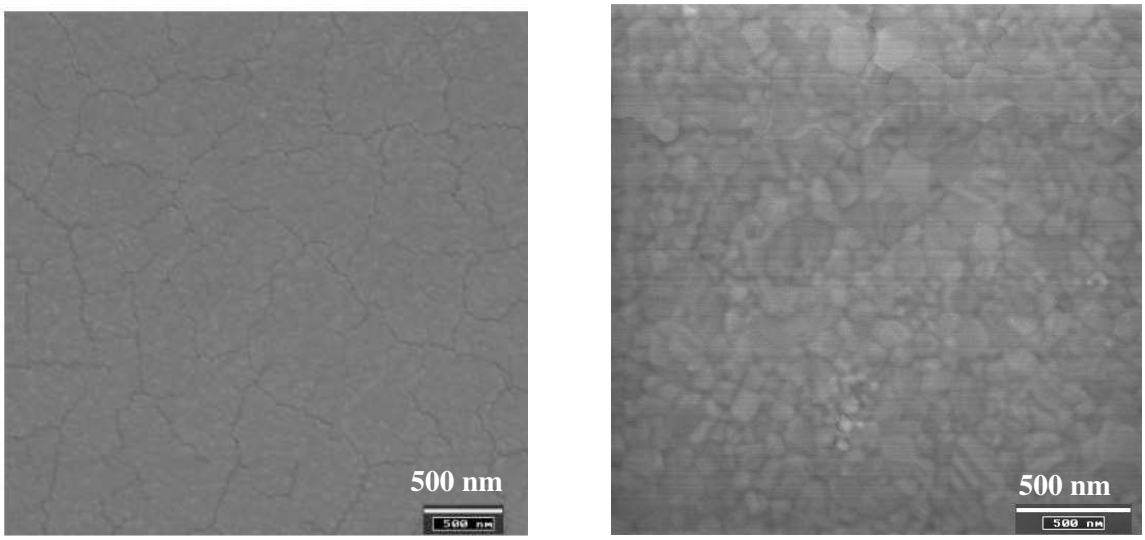


Figure 5.38 *Scheme for the preparation of BTO solution and thin film.*

The amount of 200 µl of 0.1 M BTO precursor solution was applied onto Si/Pt/$Ta_{21}Si_{57}N_{21}$ and Si/SiO_2/TiO_x/Pt(100 nm) (as reference) substrates using a spin coating process. In this one step process the film is directly heated to the crystallization temperature (700 °C) after deposition, which results in both organic removal and crystallization of $BaTiO_3$. A one-step process is more preferable for the crystallization of BTO thin films, due to its predominantly homogenous nucleation. Therefore, in order to force heterogeneous nucleation a lower solution concentration is used and each layer is directly crystallized in a diffusion oven, leading to columnar polycrystalline structures with a high dielectric constant. When using a solution concentration of 0.1 M, films of around 8 nm per layer are formed (spin speed 4000 rpm). Ten layers were deposited onto the Si/Pt/$Ta_{21}Si_{57}N_{21}$ substrate, with an expected overall thickness of 80 nm.



(a) (b)

Figure 5.39 *SEM images of top BTO thin film on a) Si/Pt/$Ta_{21}Si_{57}N_{21}$ substrate and b) Si/SiO_2/TiO_x/Pt.*

Figure 5.39 illustrates the surface morphology of BTO thin films deposited on different substrates. The columnar structure of BTO film was found on the $Ta_{21}Si_{57}N_{21}$ layer although the average grain size was smaller then on the Si/SiO_2/TiO_x/Pt substrate, indicating the heterogeneous nucleation of the dielectric film on amorphous substrate. In general, the micro structure of dielectric thin films fabricated by chemical solution deposition (CSD) process is controlled by film material, substrate interface and the processing parameters [96, 98, 99]. In the addition, the cracks in the BTO films are visible on the surface with TaSiN layer (Figure 5.39). The origin of the film cracking is usually the large volume change during the thermal treatment. The cracking is caused by excessive shrinkage of the BTO layer on the TaSiN substrate probably due to the smaller grain size.

5.3.2 Si/Pt/TaSiN/Pt/BST

The 100 nm thin $(Ba_{0.7}Sr_{0.3})TiO_3$ (BST) layer was deposited on Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt substrate by CSD using a 0.1 M BST solution. The procedure for preparing and depositing the thin dielectric film is demonstrated in Figure 5.40 and described in detail in the previous subchapter (Chapter 5.3.1).

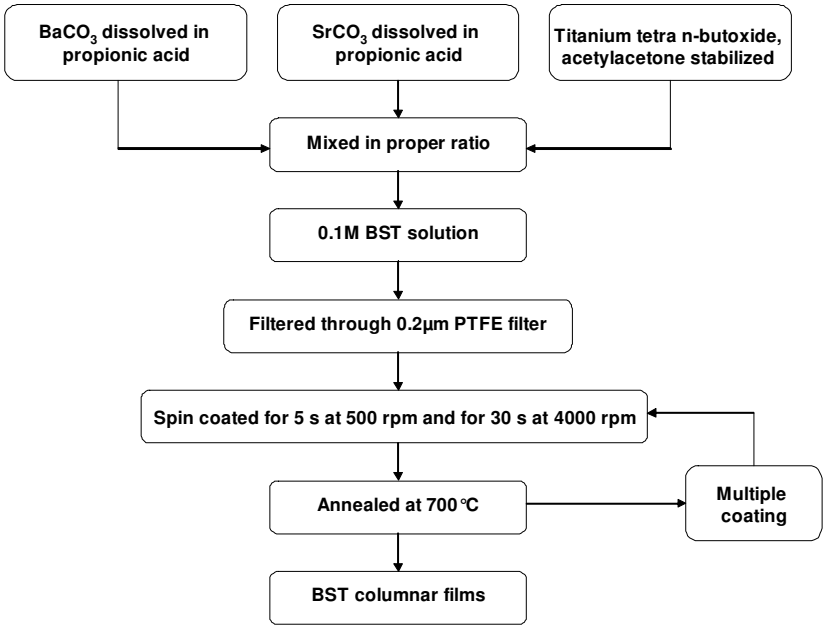
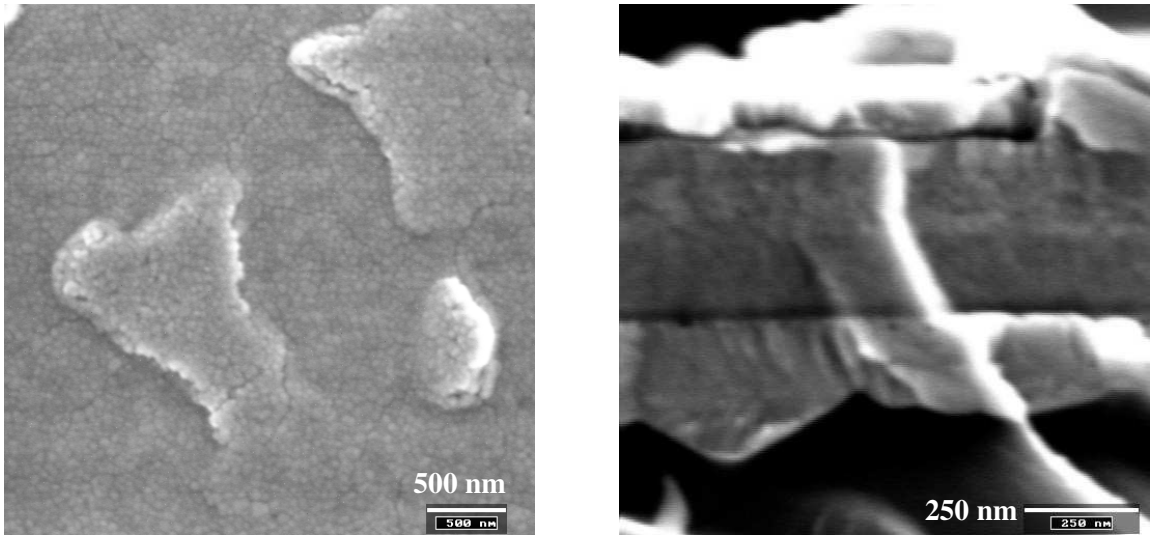


Figure 5.40 *Scheme for the preparation of BST solution and thin film.*

A fine grain structure of the dielectric layer is present after annealing the BST thin layers at 700 °C but the surface becomes very rough. The SEM picture shows the destroyed BST layer. This is probably due to the delamination of the platinum layer underneath (Figure 5.41). The rupture of the platinum top layer after several annealing steps leads to cracking and disruption in the top BST layer. Furthermore, the extremely rough platinum surface leads also to adhesion problems of BST.



(a) (b)

Figure 5.41 *SEM picture of a) top BST layer in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt/BST stack and b) sample cross section.*

CSD methods using carboxylate based routes can seldom be crystallized below 650 °C. The transition from amorphous to crystalline $BaTiO_3$ happens at temperatures between 600 °C and 650 °C. After processing at 650 °C only the reflex from $BaTiO_3$ and no carbonate bonding is visible in IR spectrum [84]. The Sr-Ti-carboxylate systems that are based on propionate routes show similar crystallization behaviour as the Ba-Ti- systems.

Lowering the deposition temperature of barium based perovskite was necessary in order to achieve the integration of the bottom electrode stack with the TaSiN layer.

Due to its quite simple concept, the pulsed laser deposition (PLD) is an attractive method for thin dielectric film fabrication of perovskite ceramics such as BTO, BST, and STO. The advantage of this method is the larger growth rate and the feasibility to optimize the deposition parameters, such as energy density, oxygen partial pressure and substrate temperature, in order to achieve the deposition of high quality crystalline thin films.

The standard parameters (pulse frequency, energy pulse and oxygen partial pressure) for the PLD deposition of BST thin films are listed in the Table 5.16 [159]. The substrate and the deposition temperature were varied. The target was a BST ceramic pellet with a Ba/Sr ratio of 70/30.

Table 5.16 *Parameters for deposition 100 nm thick $(Ba_{0.7}Sr_{0.3})TiO_3$ (BST) layer using PLD.*

Pulse frequency	10 Hz
Pulse energy	3 Jcm^{-2}
Time	2.5 min
Atmosphere	O_2
Temperature	RT, 500 °C and 550 °C

Large cracks were observed in the amorphous BST thin films deposited at room temperature on the reference sample $Si/SiO_2/TiO_x/Pt$ (Figure 5.42) [160]. No improvement was found after rapid thermal annealing in oxygen atmosphere at 550 °C for 10 minutes.

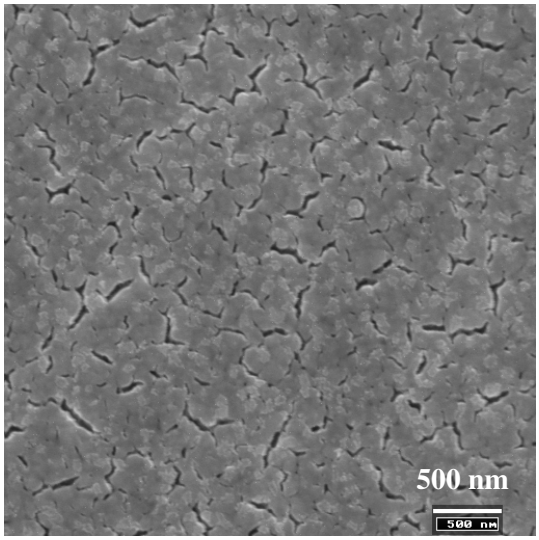


Figure 5.42 *SEM picture of BST top layer in Si/SiO_2/TiO_x/Pt/BST stack deposited at room temperature using PLD.*

The microstructure of BTO films deposited at 500 °C and 550 °C are presented in the Figure 5.43. The average grain size increases with deposition temperature (at 550 °C is ~ 100 nm). The film is dense without any visible cracks but with a porous cauliflower-like structure.

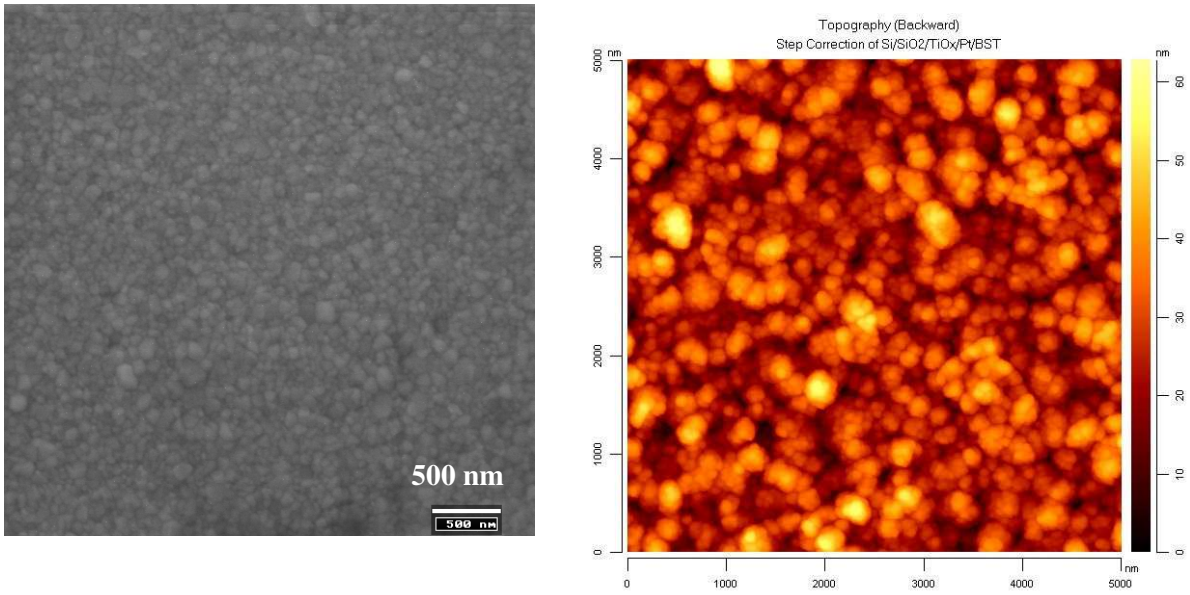


Figure 5.43 *SEM and AFM picture of BST top layer in Si/SiO_2/TiO_x/Pt/BST stack as-deposited at 550 °C using PLD.*

5.3.3 Si/Pt/TaSiN/Ir/BST

At 550 °C and the same deposition parameters as described in the Table 5.16, BST thin films were deposited on an iridium top layer in the stack Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir using PLD method.

The average grain size (~ 80 nm) is smaller than in the platinum substrate but the structure seems to be less porous (Figure 5.44).

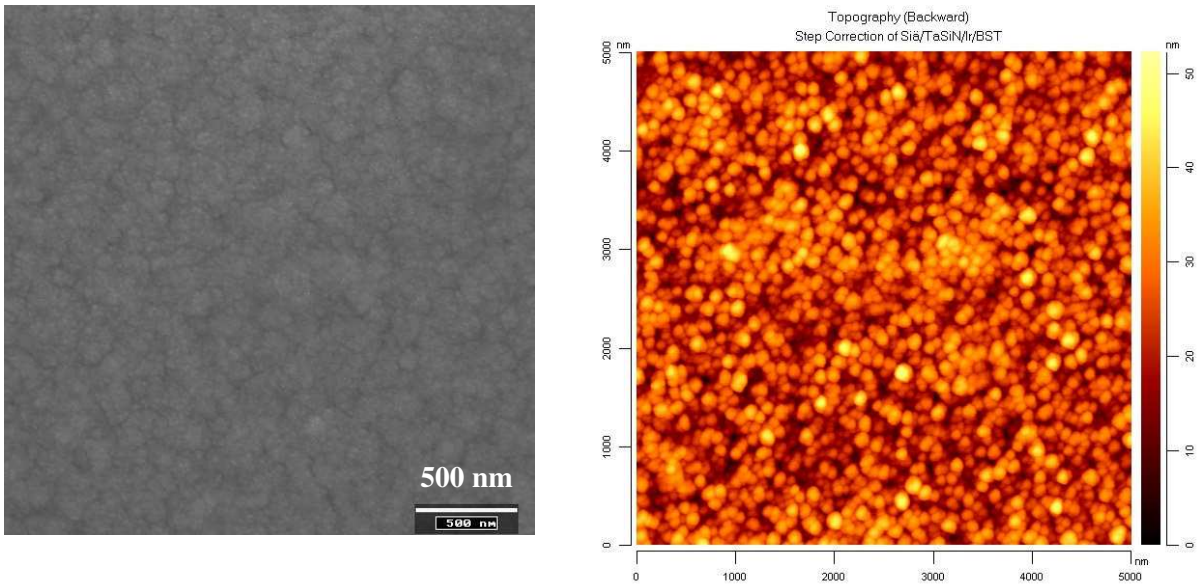


Figure 5.44 *SEM and AFM picture of BST surface after PLD deposition at 550 °C in an oxygen atmosphere on Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir sample.*

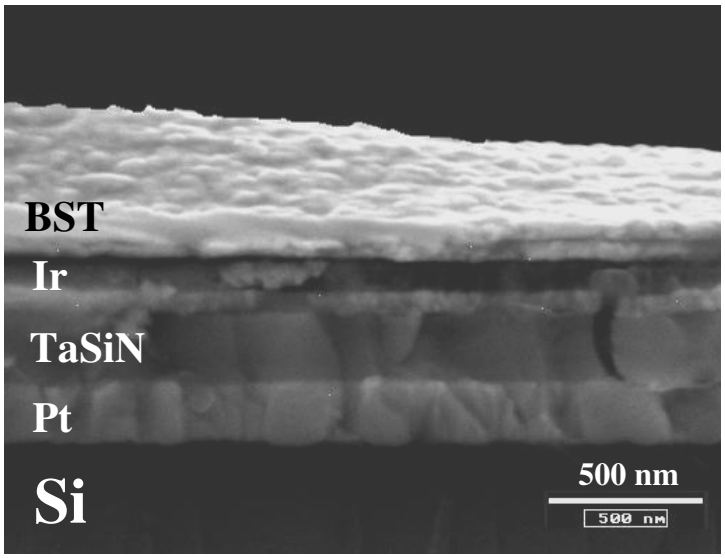


Figure 5.45 *SEM picture of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST stack cross section.*

Large BST crystal grains could be observed in the cross section of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST sample (Figure 5.45). It seems that the film consists of a BST bilayer. The X-ray diffraction diagram shows poor crystallinity in the dielectric layer with orientation (100) and (110) (Figure 5.46) which suggests that the lower layer is less crystalline and consists mostly of an amorphous phase. The upper BST layer is polycrystalline and has a columnar structure.

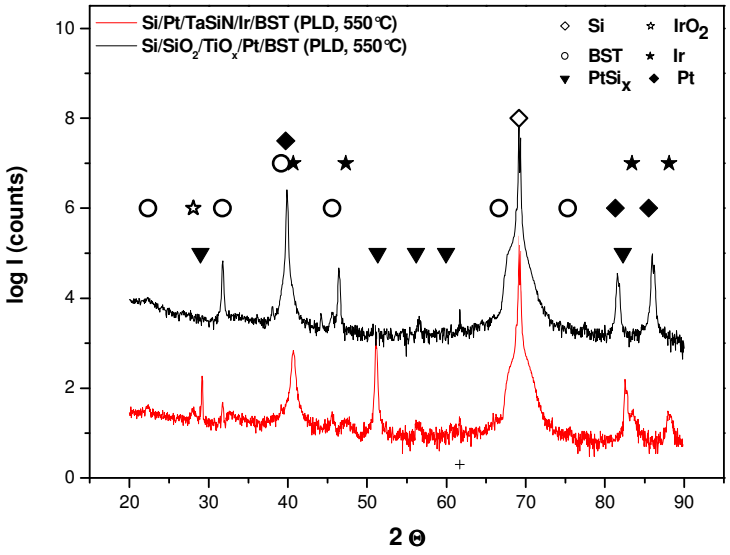


Figure 5.46 *XRD diagram for as-deposited* $Si/Pt/Ta_{21}Si_{57}N_{21}/Ir/BST$ *and* $Si/SiO_2/TiO2/Pt/BST$ *stacks (BST: PLD at 550 °C).*

The Ba/Sr and Ti/(Ba+Sr) ratio of polycrystalline BST layer, measured by XRF, was 65/35 and 1.11, respectively. The change in the composition of the BST layer is attributed to the substrate temperature which is lower then the BST crystallization temperature (700 °C). The nucleation of a film is determined by the equilibrium between the vapour and the solid phases of the material ejected from the target [138]. The equilibrium vapour pressure is temperature dependent. When the vapour pressure of the arriving particles is larger then its equilibrium value, it is energetically favourable for the vapour to condense onto the substrate.

5.4 Dielectric properties of capacitors

5.4.1 Electrical permittivity

Once the dielectric films are deposited and crystallized (in a diffusion oven for films deposited by CSD), electrodes were deposited on the layer in order to electrically characterize the metal-insulator-metal (MIM) stack. The top electrodes (TE) were formed by a "lift-off" process. First the dielectric films were covered with a negative photo-resist layer, patterned with a mask by exposure to UV light and finally developed. Platinum is then sputtered or vacuum evaporated at room temperature making the desired TE in the developed areas. The undeveloped parts were then dissolved in acetone. The sample was rinsed in isopropanol and dried in a nitrogen gas stream. The process is outlined schematically in Figure 5.47.

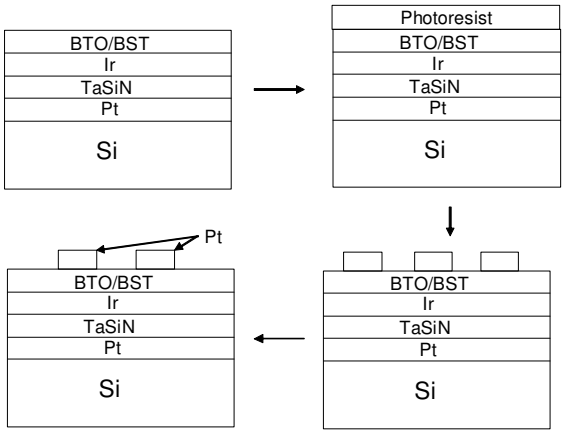


Figure 5.47 *Schematic presentation for the fabrication of MIM structures.*

After deposition of top platinum electrodes, the films were rapid thermal annealed at 500 °C in an oxygen atmosphere to ensure better contact between the top electrode and the surface of the dielectric layer.

The capacitance of the thin film capacitor was measured at different bias voltages with the precision LCR meter HP4284A from Hewlett Packard. The standard characterization was performed at 1 kHz in order to avoid a frequency resonance at 500 kHz and low frequency (50 Hz) interference with the power supply voltage (220 V). The sample capacitance was measured as a function of the bias voltage, i.e. a so called *C(V)* characteristic. Additionally, the frequency dependence of capacitance was examined.

At first, the BTO thin film deposited by CSD was characterized. The reference sample $Si/SiO_2/TiO_x/Pt/BTO/Pt_{(top)}$ was used to compare the measured data for the $Si/Pt/Ta_{21}Si_{57}N_{21}/BTO/Pt_{(top)}$ stack.

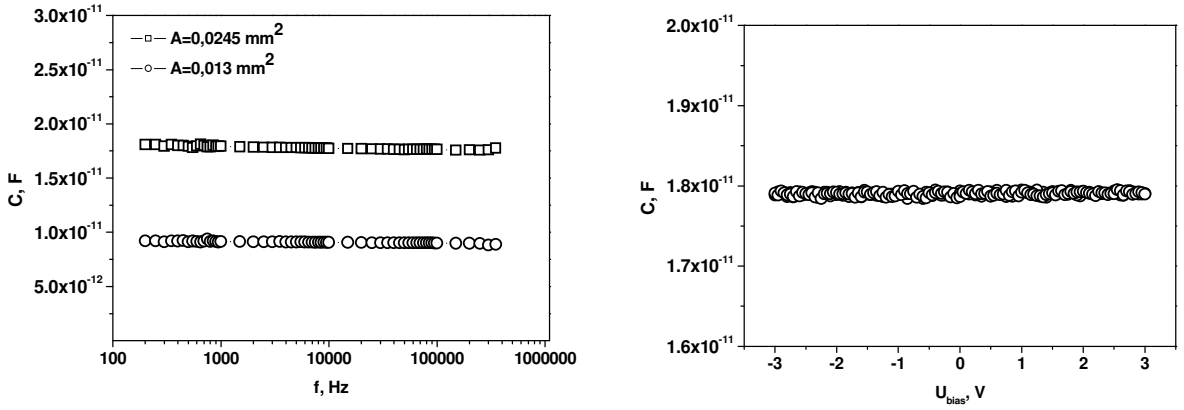


Figure 5.48 *a) C-f and b) C-U measurement of $Si/Pt/TaSiN_{(bottom)}/BTO/Pt_{(top)}$ stack with electrode area A = 0.0245 mm^2 at room temperature and an oscillation frequency f = 1 kHz.*

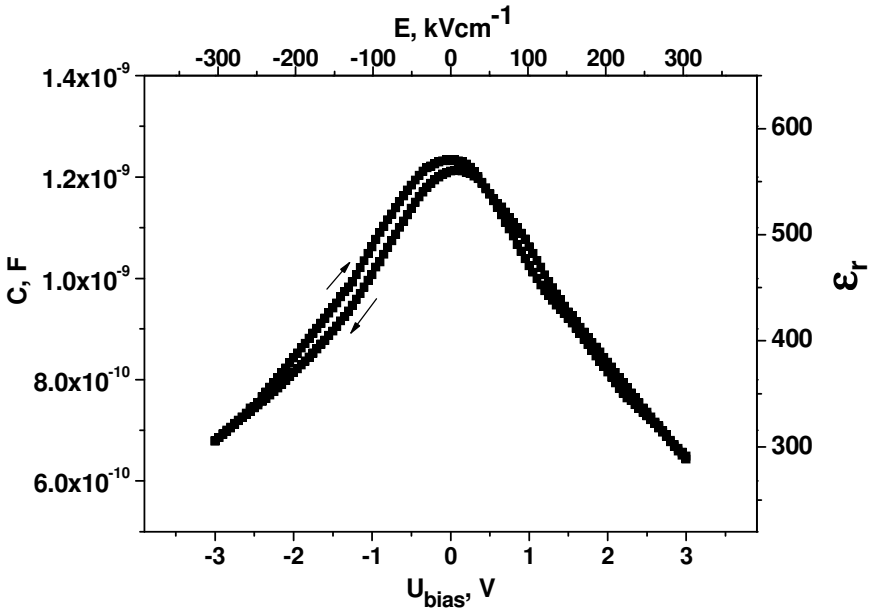


Figure 5.49 *Capacitance and permittivity dependence on bias voltage for reference sample $Si/SiO_2/TiO_x/Pt_{(bottom)}$ /BTO/$Pt_{(top)}$ at room temperature and oscillation frequency f = 1 kHz for electrode area A = 0.0245 mm^2.*

The capacitance of the reference sample is two orders of magnitude larger then for the stack $Si/Pt/Ta_{21}Si_{57}N_{21}/BTO/Pt_{(top)}$ and the calculated permittivity is ~ 600 (Figure 5.48 and Figure 5.49). The calculated permittivity of BTO layer (from equation 4.28) in the stack with TaSiN layer is ~ 8. That indicates a parallel connection of BTO layer and/or one unknown layer (dead layer) with a low capacitance (Figure 5.50), because the overall capacitance *C* is determined by the lower one C_x:

$$\frac{1}{C} = \frac{1}{C_X} + \frac{1}{C_{BTO}} \approx \frac{1}{C_X} \tag{5.7}$$

$$\left(\frac{d}{\varepsilon_r}\right)_X = \frac{\varepsilon_0 A}{C} - \frac{d_{BTO}}{\varepsilon_{r,BTO}} \approx 12nm \tag{5.8}$$

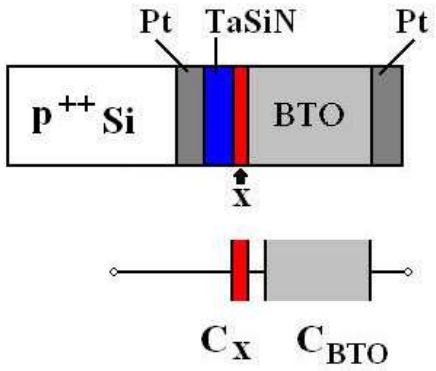


Figure 5.50 *Equivalent circuit in the case of serial connection of BTO and unknown dielectric layer X (dead layer).*

As the TaSiN thin layer failed as a bottom electrode, an iridium thin film was introduced between the TaSiN and the dielectric thin film. Afterwards, the BST thin film was deposited using the PLD at 550 °C. Finally, the platinum top electrodes were sputtered in order to fabricate the capacitor system. At the first, the BST layer was characterized when deposited using PLD at a lower temperature on the reference sample. As in the previous measurement, the capacitance of the reference capacitor system, $Si/SiO_2/TiO_x/Pt/BST/Pt_{(top)}$, was measured and the corresponding permittivity was calculated, based on the thin film thickness. The permittivity of amorphous BST layer after deposition at 500 °C and annealing at 550 °C is only 120 (Figure 5.51). The BST layers deposited at 550 °C show much higher permittivity (ε_r ~ 430).

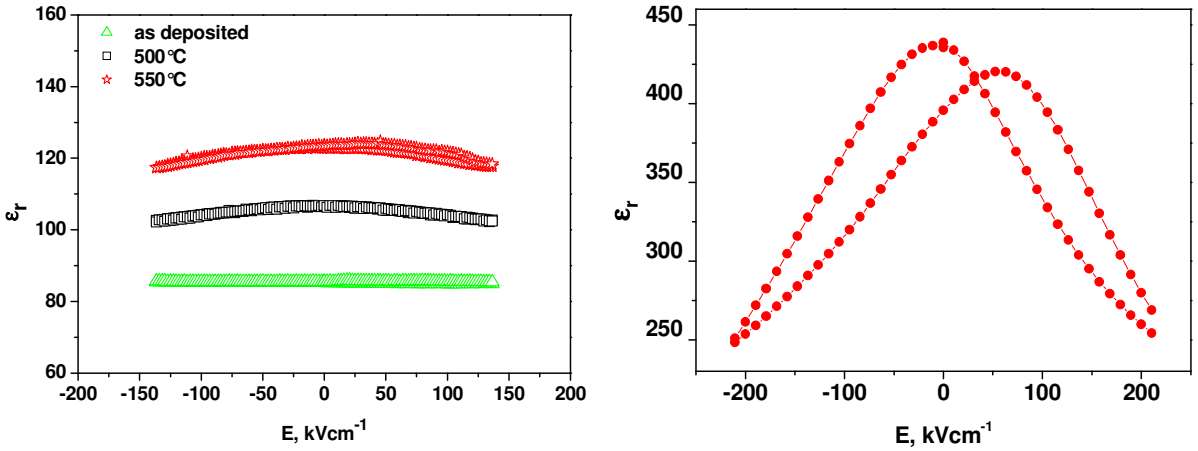


Figure 5.51 *Permittivity of BST thin film (a) deposited using PLD at 500 °C and then annealed at indicated temperatures in an O_2 atmosphere and (b) deposited at 550 °C and annealed at the same temperature in an O_2 atmosphere.*

Finally, the $Si/Pt/Ta_{21}Si_{57}N_{21}/Ir/BST/Pt_{(top)}$ stack was characterized. The electrical contact with the bottom electrode could be made in two different ways. Etching a small part of BST layer uncovered a small part of the iridium electrode for contact making an $Ir/BST/Pt_{(top)}$ MIM capacitor stack. In this application, the highly doped p^{++}-silicon wafer should serve as the bottom electrode, so the electrical contact was made from the back side of silicon*. Prior to platinum deposition, the small part on the backside of the silicon wafer was etched in order to remove the native silicon dioxide. After that, it was bonded to a copper plate making an electrical contact with the silicon (Figure 5.52).

* See the Figure 1.7

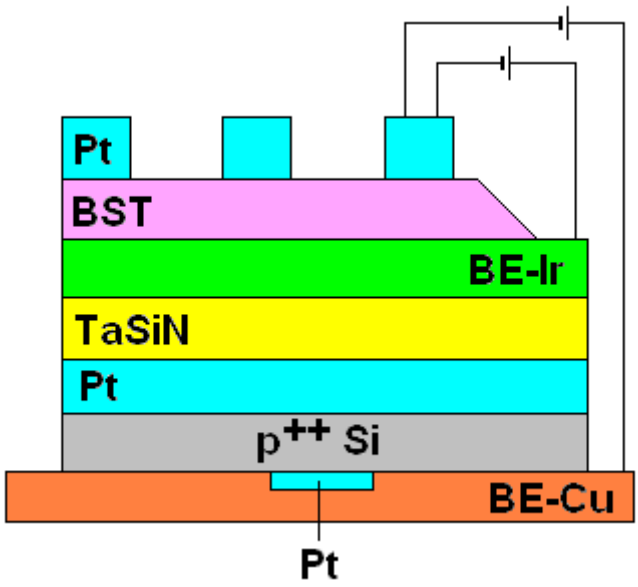


Figure 5.52 *Scheme of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt(top) stack used for a electrical characterisation for two different measurement: a) Ir bottom electrode (BE – Ir) and b) Cu bottom electrode (BE – Cu).*

The permittivity of the BST thin film in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt(top) is ~ 470 and reaches its maximum at ± 20 mV (Figure 5.53). There is no difference if the electrical contact with bottom electrode was made to the intermediate electrode iridium or to the copper plate through the whole stack.

The *C-V* curve has a "butterfly" shape, which may indicate the ferroelectric property of the BST film.

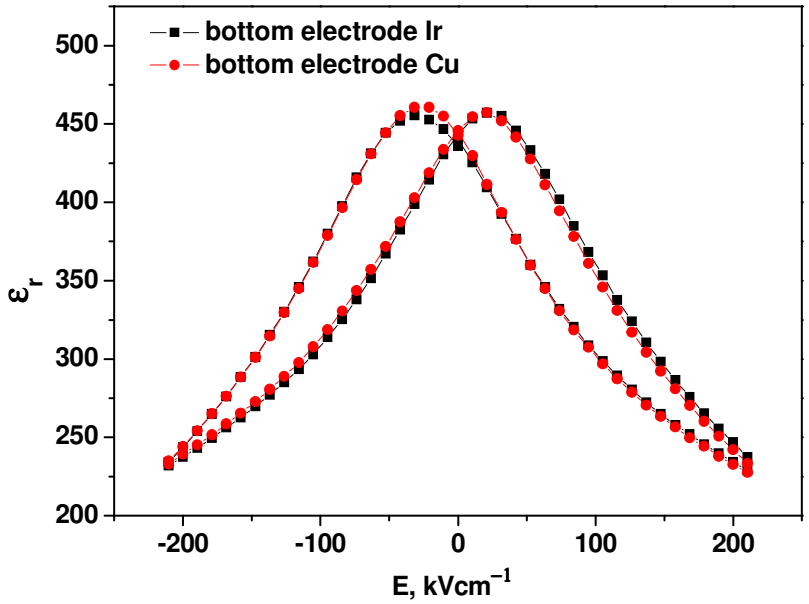


Figure 5.53 *Permittivity for the BST thin film in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt(top) stack after deposition at 550 °C and annealing at the same temperature in O_2.*

5.4.2 Leakage current

Among other parameters such as fast dielectric response and long life time, leakage current is an important parameter for the quality and reliability of devices with dielectric and ferroelectric thin films. When a voltage step V is applied to a dielectric thin film at the time $t = 0$, the current response in the time regime can be schematically divided into three regimes: relaxation, leakage and degradation regime (Figure 5.54). In the relaxation regime the current decreases continuously with time ($j(t) \sim t^{-0.66}$) and during the leakage regime the current is $J_L = \text{const}$. When the current begins to increase, the degradation regime starts. The time at which the resistance has decreased by a factor of ten (corresponding to a current increase of 10x at constant applied voltage) is called the life time of dielectric material. Ideally, the leakage current or steady state current is time independent and represented with a plateau. The leakage current and the length of the plateau depend strongly on electrical field, temperature and material parameters. However, in general, the rules states that the lower the leakage current, the longer the relaxation regime. At lower measurement temperatures and a low electrical field, the leakage current minimum may be reached after more then 10^4 s. On the other hand, at higher temperatures and high electrical fields, the leakage current minimum may appear after a very short time span, even below 1 s. Therefore, measurements at constant time, preferentially short times (as frequently reported in literature) give rise to large errors in leakage current determination.

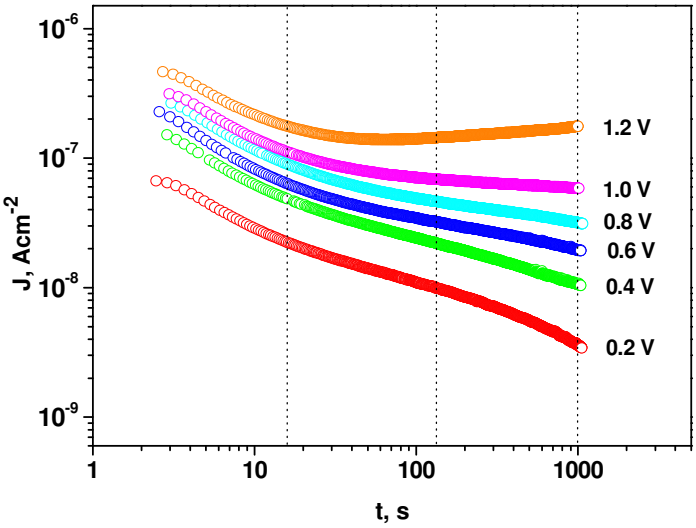


Figure 5.54 *Current response of BST thin film in a Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt stack upon voltage step stimulation.*

The leakage current dependence on the electrical field was measured by applying the voltage with 0.1 V step, as shown in Figure 5.55. After applying the voltage the current was recorded for 300 s. Then, the sample was first depolarised ($V = 0$) also for 300 s and the next voltage

step was applied. At lower voltages ($U \leq 0.6$ V), the leakage current plateau was not reached after 300 s (Figure 5.54). Therefore, the displayed leakage current in the Figure 5.55 for the voltages less then 0.6 V are slightly overestimated [126].

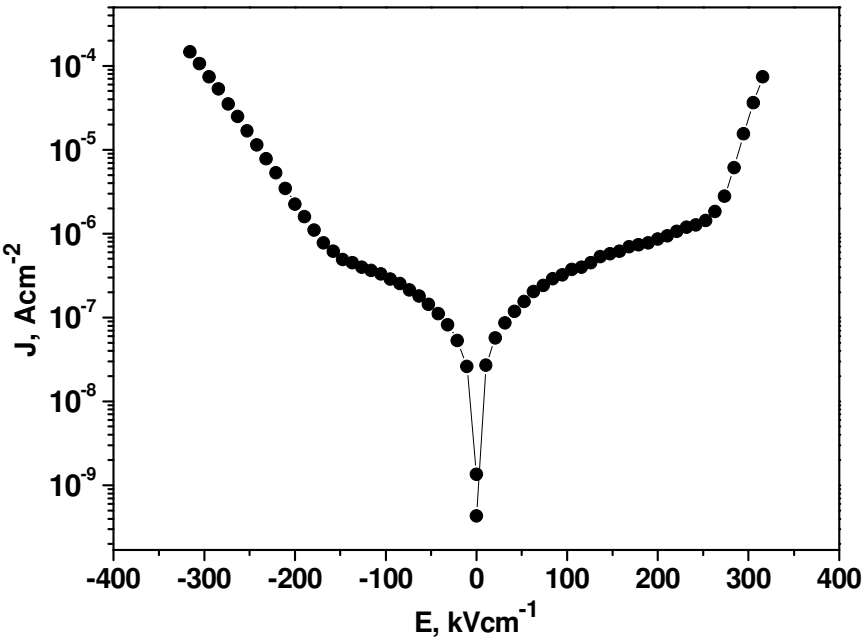


Figure 5.55 *Leakage current for BST in Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt(top) stack after deposition at 550 °C and annealing at the same temperature in O_2 (BE-Ir).*

The leakage current density-electrical field characteristic ($logI - E$) of the capacitor system Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt, for which the top electrode was platinum and the bottom electrode the highly doped p^{++}-silicon, connected to a copper plate, is shown in Figure 5.55. (the BST thickness was 100 nm and the electrode area was 0.245 mm^2). By increasing the electrical field values from 50 $kVcm^{-1}$ up to 200 $kVcm^{-1}$ the current density increases slowly and is lower then $1 \cdot 10^{-6}$ Acm^{-2}. With larger electrical fields the leakage current density dramatically increases nearly exponentially.

The asymmetric behaviour of leakage current is attributed to the different top and bottom electrodes.

5.4.3 Large signal hysteresis measurement

This section deals with determining the hysteresis loops using polarization vs. voltage measurements. In order to measure the whole stack, the bottom side of the p^{++}-Si wafer was coated with 100 nm thick platinum layer and fixed with silver paste on a copper plate, which

served as bottom electrode*. The measurements were performed on BST films deposited at 550 °C using PLD on a sample with iridium (Si/Pt/$Ta_{21}Si_{57}N_{21}$/**Ir**/BST/Pt(top)) and copper (**Cu**-Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt(top)) bottom electrodes and on a reference sample (Pt/BST/Pt) (Figure 5.56). The frequency used in these measurements was 100 Hz, resulting in reduced leakage currents.

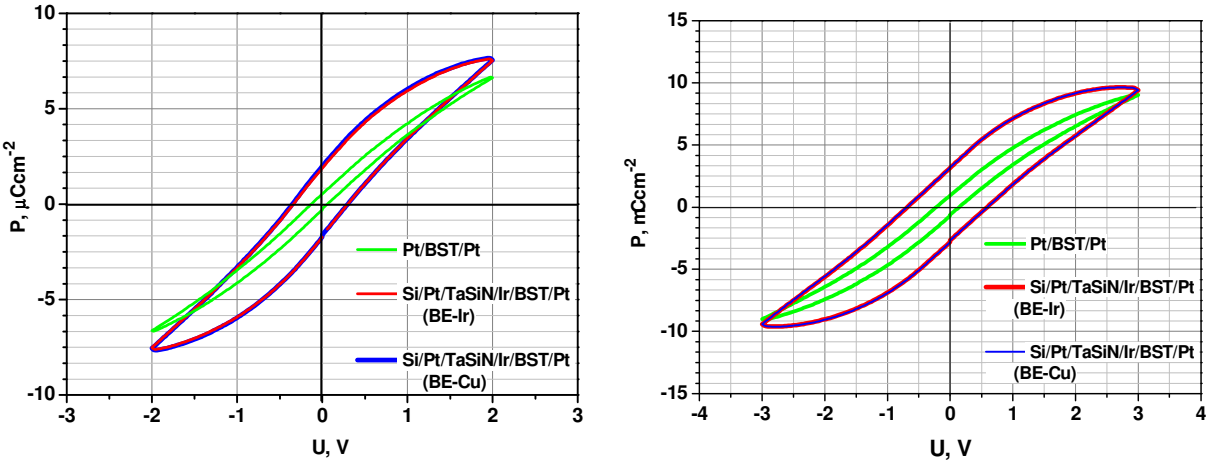


Figure 5.56 *Polarisation measurements vs. applied voltage (at f = 100 Hz) for BST in (**Cu**-Si/Pt/$Ta_{21}Si_{57}N_{21}$/**Ir**/BST/Pt(top) and Pt/BST/Pt stacks after deposition and annealing at 550 °C in O_2: (a) 2 V and (b) 3 V.*

No difference was observed regarding the measurements performed on the bottom iridium electrode and on the copper plate attached to the backside of the highly doped p^{++}-silicon wafer

For a 130 nm thick BST film prepared using PLD at 700 °C the phase transition temperature para- to ferroelectric is 17 °C. Above this temperature the BST film is in the paraelectric phase [159]. As many non-ferroelectric materials systems show a pseudo-ferroelectricity [160-163], i.e. a ferroelectric-like hysteresis in $C-V$ and $P-E$ loops, the identification of a ferroelectric behaviour has to be carefully analyzed, especially in the presence of slow kinetic effects, long relaxation times and higher leakage currents.

The commercially available apparatus for hysteresis measurement uses charge or current integration. For an ideal ferroelectric insulator the polarisation can be calculated from switched charge ΔQ:

$$\Delta Q = 2P_r A \tag{5.9}$$

* See the Figure 1.7

where P_r is the remanent polarisation, and A is the electrode area for a parallel-plate capacitor. For real ferroelectric, the switched charge is given by:

$$\Delta Q = 2P_r A + \sigma EAt \tag{5.10}$$

where σ is the electrical conductivity, E is the applied field, and t the measuring time. For a ferroelectric material the second term should be lower then the first. Furthermore, in the case of non-ferroelectric material ($P_r = 0$) ΔQ is not zero:

$$\Delta Q = \sigma EAt \tag{5.11}$$

This equation describes a lossy linear dielectric. Even linear lossy dielectrics can show $P-E$ hysteresis loop, as shown in Figure 5.56. Such behaviour has nothing with polarisation or ferroelectricity.

6 Summary and conclusions

6.1 Summary

The goal of this work was to develop a conductive oxygen diffusion barrier for the processing of high-κ materials (BST or BTO) on good conducting, highly p-doped silicon wafers (p^{++}-Si) which are used as a bottom electrode in the metal-insulator-metal (MIM) thin film capacitor stack. The thesis consists of two parts: the optimisation of Ta-Si-N composition for use as oxygen diffusion barrier and the electrical characterisation of p^{++}-Si – diffusion barrier – high-κ material – metal stack.

TaSiN was deposited using reactive rf-magnetron sputtering technique in a nitrogen atmosphere at room temperature and 500 °C. In order to achieve different $Ta_xSi_yN_z$ composition the cathode power and the nitrogen flow ratio were varied and two different $TaSi_x$ targets ($x = 1$ and 2.7) were used. The film composition was determined using Rutherford backscattering spectroscopy. The results can be summarized:

- TaSiN films deposited in an N_2 + Ar gas mixture with N_2 to N_2 + Ar flow ratio of 10 % for all cathode power were insulating. Using a 0.1 % $N_2/(N_2 + Ar)$ flow ratio and different cathode power, the composition of TaSiN thin films were $Ta_{22}Si_{22}N_{54}$ (120 W), $Ta_{28}Si_{28}N_{43}$ (180 W) and $Ta_{33}Si_{33}N_{33}$ (240 W) using TaSi target and $Ta_{15}Si_{44}N_{41}$ (120 W), $Ta_{19}Si_{54}N_{26}$ (180 W) and $Ta_{21}Si_{57}N_{21}$ (240 W) for $TaSi_{2.7}$ target. No difference in stoichiometry was observed for the films deposited at room temperature and at 500 °C. Therefore, room temperature was set as the standard deposition temperature.
- The as-deposited TaSiN films are amorphous. The crystallisation temperature of thin TaSiN films was defined as temperature at which the polycrystalline $TaSi_2$ phase was formed and could be identified using XRD technique. In all the compositions, it was determined the crystallisation temperature was in the range from 750 °C to 1000 °C and increased with higher nitrogen content.

- Following deposition and annealing processes at 700 °C, the sheet resistance was measured using the four point probe method. The as-deposited films have metallic conduction with Ohmic behaviour. The resistivity of as-deposited films with different compositions depends on the nitrogen content and ranges from 10^{-6} Ωm to 10^{-3} Ωm. After annealing at 700 °C for 10 minutes in an oxygen atmosphere, the TaSiN layers that have higher nitrogen and lower silicon content were insulating. Hence, the samples with same nitrogen but different silicon content show a different behaviour.

Through this methodology, it could be determined that the p^{++}-Si/TaSiN junction develops unacceptable contact resistance. Further progresses were made:

- By introducing an intermediate Pt layer (100 nm), the p^{++}-Si/Pt/TaSiN stack had good conductive properties and good thermal stability at 700 °C. Above 500 °C, the thin platinum layer reacted completely with the Si substrate forming conductive platinum-silicides (PtSi, Pt_2Si, Pt_3Si), detected using X-ray diffraction. The deposition of high-κ material directly on the TaSiN surface and subsequently annealing in the oxygen atmosphere at 700 °C resulted in the reduction of the overall capacity.
- An additional platinum protective layer did not improve the stack p^{++}-Si/Pt/TaSiN/Pt behaviour after annealing at elevated temperature (except for $Ta_{28}Si_{28}N_{43}$ and $Ta_{33}Si_{33}N_{33}$). Moreover, when the temperature rose above 500 °C, the roughness was unacceptably high in all samples (*rms* above 5 nm).
- By introducing an iridium layer, the thermal properties of the p^{++}-Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir stack improved (except for $Ta_{15}Si_{44}N_{41}$). Once again, at temperatures exceeding 600 °C, the roughness became unacceptably high (*rms* above 30 nm). After annealing at 550 °C, the Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir stack remained conductive. And, the roughness measured on the top layer was less than 1 nm, thus acceptable for the further implementation.

The BST layer was deposited using PLD at 550 °C on the Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir stack. For the electrical measurement a top Pt layer was deposited by DC magnetron sputtering and subsequently structured by a lift-off lithographic process. In order to measure the whole stack, the bottom side of the p^{++}-Si wafer was coated with 100 nm thick platinum layer and fixed with silver paste on a copper plate which served as the bottom electrode. The samples demonstrated low capacitance, leakage current and the ferroelectric polarization of the samples have been found:

- In an electrical field near to zero, the dielectric constant is $\kappa \approx 470$. The capacitance – electrical field dependence has a slight butterfly shape which may indicate some ferroelectricity in the thin BST film and the curve is largely tunable.

- The leakage current is not completely symmetric due to the different top and bottom electrodes, platinum and p^{++}-Si, respectively. The absolute current is below 10^{-6} A/cm^2 for fields lower than ± 200 kV/cm corresponding to an applied voltage of ± 2 V.
- The hysteresis loops were determined by measuring the polarization vs. voltage on a sample with iridium (Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt(top)) and copper (Cu-Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt(top)) bottom electrodes. BST thin films, deposited using PLD at 550 °C, show a ferroelectric-like hysteresis in $C-V$ and $P-E$ loops, especially in the presence of slow kinetic effects, long relaxation times and higher leakage currents.

6.2 Conclusions

In the scope of this research the composition of TaSiN thin films was successfully optimised for the application as oxygen diffusion barrier for the deposition of high-κ materials. TaSiN thin films have promising behaviour, considering that thin films are amorphous, and thus free from fast diffusion paths, conductive and thermally stable at temperature needed for deposition of perovskite dielectrics. The integration of TaSiN in stack capacitor systems brings several difficulties. The deposition of high-κ material directly on the TaSiN surface resulted in the reduction of the overall capacity. The introduction of protective platinum or iridium layer on top of TaSiN improves the thermal behaviour of the p^{++}-Si/Pt/TaSiN/Ir stack but induces an unacceptably high roughness at temperatures exceeding 600 °C. The dielectric properties of Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir/BST/Pt are reasonable and suitable for the biological application compared to the used dielectrics. Moreover, the leakage current is below 10^{-6} A/cm^2 for fields lower than ± 200 kV/cm, which is acceptable for DRAM applications.
The existing integration scheme of TaSiN in capacitor system has to be further developed, in order to withstand the standard processing temperature of perovskite materials.

Appendix

A.1 Identification of phases from XRD diagram for different samples

Table A.1.1 *Qualitative phase analysis for hexagonal $TaSi_2$ crystallized after annealing $Ta_{21}Si_{57}N_{21}$ thin film at 750 °C.*

2θ, measured	2θ, JCPDS* (Intensity, %)	Reflex
21.612	21.426 (15)	(100)
25.606	25.396 (100)	(101)
34.993	34.830 (54)	(102)
37.554	37.556 (14)	(110)
40.093	40.096 (84)	(111)
41.504	41.182 (27)	(003)
43.651	43.669 (29)	(200)
46.961	46.961 (59)	(112)
61.634	61.584 (17)	(203)
66.132	66.041 (9)	(212)
69.545	69.512 (28)	(301)

*Joint Committee on Powder Diffraction Standards

Table A.1.2 *Identification of phases from XRD diagram for Si/Pt/$Ta_{21}Si_{57}N_{21}$sample as-deposited and after annealing using JCPDS data.*

Phase	2θ, measured			2θ, JCPDS (Intensity, %)	Reflex
As-deposited					
Pt	39.709			39.766 (100)	(111)
Si (substrate)	69.130			69.130 (100)	(400)
Pt	81.428			81.286 (33)	(311)
Pt	85.416			85.712 (12)	(222)
After annealing					
	500 °C	600 °C	700 °C		
PtSi	29.156	29.193	29.133	28.966 (90)	(101)
PtSi	51.004	51.102	51.056	51.314(30)	(130)
Pt_2Si	56.082	56.193	56.185	56.177 (35)	(202)
PtSi	60.389	60.490	60.447	59.938 (30)	(202)
Si (substrate)	69.130	69.130	69.130	69.130 (100)	(400)
Pt_3Si	82.409	82.566	82.526	82.264 (80)	(311)

Table A.1.3 *Identification of phases from XRD diagram for Si/Pt sample as-deposited and after annealing using JCPDS data.*

Phase	2θ, measured			2θ, JCPDS (Intensity, %)	Reflex
As-deposited					
Pt	39.760			39.766 (100)	(111)
Si (substrate)	69.130			69.130 (100)	(400)
Pt	81.331			81.286 (33)	(311)
Pt	85.561			85.712 (12)	(222)
After annealing					
	500 °C	600 °C	700 °C		
PtSi	29.156	29.193	29.133	28.966 (90)	(101)
Pt	39.852	39.739	39.675	39.766 (100)	(111)
PtSi	51.004	51.102	51.056	51.314(30)	(130)
Pt_2Si	56.082	56.193	56.185	56.177 (35)	(202)
PtSi	60.389	60.490	60.447	59.938 (30)	(202)
Si (substrate)	69.130	69.130	69.130	69.130 (100)	(400)
Pt_3Si	82.409	82.566	82.526	82.264 (80)	(311)

Table A.1.4 *Identification of phases from XRD diagram for Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt sample as-deposited and after annealing using JCPDS data.*

Phase	2θ, measured			2θ, JCPDS (Intensity, %)	Reflex
As-deposited					
PtSi	30.058			30.063 (50)	(200)
Pt	39.832			39.766 (100)	(111)
Pt_2Si	44.694			44.692 (100)	(112)
Pt	46.230			46.243 (53)	(200)
Pt_2Si	56.053			56.177 (35)	(202)
Si (substrate)	69.130			69.130 (100)	(400)
Pt	81.080			81.286 (33)	(311)
Pt	85.703			85.712 (12)	(222)
After annealing					
	500 °C	600 °C	700 °C		
PtSi	29.211	29.374	29.236	28.966 (90)	(101)
PtSi	/	30.177	30.094	30.063 (50)	(200)
Pt_2Si	32.236	32.148	31.894	32.124 (90)	(110)
Pt	39.803	39.994	39.830	39.766 (100)	(111)
PtSi	/	42.904	42.782	42.569 (80)	(211)
PtSi	/	43.919	43.764	43.582 (100)	(121)
Pt_2Si	44.781	/	/	44.692 (100)	(112)
Pt	46.266	/	/	46.243 (53)	(200)
PtSi	51.105	51.341	51.203	51.314 (50)	(130)
Pt_2Si	56.258	56.427	56.294	56.177 (35)	(202)
PtSi	60.638	60.627	60.494	59.938 (30)	(202)
Si (substrate)	69.130	69.130	69.130	69.130 (100)	(400)
Pt_3Si	82.491	82.747	82.635	82.264 (80)	(311)
Pt	85.955	85.902	85.761	85.712 (12)	(222)

Table A.1.5 *Identification of phases from XRD diagram for Si/Pt/$Ta_{33}Si_{33}N_{33}$/Pt sample as-deposited and after annealing using JCPDS data.*

Phase	2θ, measured			2θ, JCPDS (Intensity, %)	Reflex
As-deposited					
Pt	39.730			39.766 (100)	(111)
Si (substrate)	69.130			69.130 (100)	(400)
Pt	81.450			81.286 (33)	(311)
Pt	85.610			85.712 (12)	(222)
After annealing					
	500 °C	600 °C	700 °C		
PtSi	29.080	29.080	29.130	28.966 (90)	(101)
Pt	39.790	39.830	39.850	39.766 (100)	(111)
Pt	46.385	/	/	46.243 (53)	(200)
PtSi	50.930	51.030	51.130	51.314(30)	(130)
Pt_2Si	56.180	56.130	56.320	56.177 (35)	(202)
PtSi	/	60.480	60.530	59.938 (30)	(202)
Si (substrate)	69.130	69.130	69.130	69.130 (100)	(400)
Pt_3Si	82.380	82.540	82.570	82.264 (80)	(311)
Pt	85.880	85.980	86.010	85.712 (12)	(222)

Table A.1.6 *Identification of phases from XRD diagram for Si/Pt/$Ta_{28}Si_{28}N_{42}$/Pt sample as-deposited and after annealing using JCPDS data.*

Phase	2θ, measured			2θ, JCPDS (Intensity, %)	Reflex
As-deposited					
Pt	39.730			39.766 (100)	(111)
Pt	46.170			46.243 (53)	(200)
Si (substrate)	69.130			69.130 (100)	(400)
Pt	81.450			81.286 (33)	(311)
Pt	85.610			85.712 (12)	(222)
After annealing					
	500 °C	600 °C	700 °C		
PtSi	29.080	29.080	29.130	28.966 (90)	(101)
Pt	39.790	39.830	39.890	39.766 (100)	(111)
Pt	46.385	/	/	46.243 (53)	(200)
PtSi	50.980	51.030	51.170	51.314(30)	(130)
Pt_2Si	56.130	56.180	56.240	56.177 (35)	(202)
PtSi	/	60.430	60.530	59.938 (30)	(202)
Si (substrate)	69.130	69.130	69.130	69.130 (100)	(400)
Pt_3Si	82.380	82.540	82.610	82.264 (80)	(311)
Pt	85.880	85.980	86.010	85.712 (12)	(222)

Table A.1.7 *Identification of phases from XRD diagram for Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ta/Pt (1) and Si/Pt/$Ta_{21}Si_{57}N_{21}$/Pt (2) sample as-deposited and after annealing at 700 °C using JCPDS data.*

Phase	2θ, measured		2θ, JCPDS (Intensity, %)	Reflex
As-deposited	(1)	(2)		
PtSi	/	30.058	30.063 (50)	(200)
Pt	39.810	39.832	39.766 (100)	(111)
Pt_2Si	/	44.694	44.692 (100)	(112)
Pt	/	46.230	46.243 (53)	(200)
Pt_2Si	/	56.053	56.177 (35)	(202)
Si (substrate)	69.130	69.130	69.130 (100)	(400)
Pt	81.373	81.080	81.286 (33)	(311)
Pt	85.702	85.703	85.712 (12)	(222)
After annealing at 700 °C	(1)	(2)		
PtSi	29.218	29.236	28.966 (90)	(101)
PtSi	30.196	30.094	30.063 (50)	(200)
PtSi	32.005	31.894	31.983 (90)	(020)
Pt	39.847	39.830	39.766 (100)	(111)
PtSi	42.823	42.782	42.569 (80)	(211)
PtSi	43.874	43.764	43.582 (100)	(121)
PtSi	48.909	/	48.734 (60)	(310)
PtSi	51.189	51.203	51.134 (50)	(130)
Pt_2Si	56.245	56.294	56.177 (35)	(202)
PtSi	60.571	60.494	59.938 (30)	(202)
Si (substrate)	69.130	69.130	69.130 (100)	(400)
Pt_3Si	82.631	82.635	82.264 (80)	(311)
Pt	85.897	85.761	85.712 (12)	(222)

Table A.1.8 *Identification of phases from XRD diagram for Si/Pt/$Ta_{21}Si_{57}N_{21}$/Ir sample as-deposited and after annealing using JCPDS data*

Phase	2θ, measured				2θ, JCPDS (Intensity, %)	Reflex
As-deposited						
Pt	39.767				39.766 (100)	(111)
Si (sub.)	69.130				69.130 (100)	(400)
Pt	85.555				85.712 (12)	(222)
After annealing						
	500 °C	550 °C	600 °C	700 °C		
IrO_2	/	/	/	27.866	28.054 (100)	(110)
PtSi	29.308	29.175	29.179	29.053	28.966 (90)	(101)
IrO_2	/	/	/	34.624	34.714 (90)	(101)
Ir	40.721	40.485	40.680	40.543	40.660 (100)	(111)
Ir_2Si	/	/	47.180	47.024	47.165 (5)	(102)
PtSi	51.198	51.085	51.118	51.022	51.314 (30)	(130)
Pt_2Si	56.221	56.085	56.271	56.074	56.177 (35)	(202)
PtSi	/	/	/	60.435	59.938 (30)	(202)
Si(sub.)	69.130	69.130	69.130	69.130	69.130 (100)	(400)
Pt_3Si	82.585	82.435	82.536	82.455	82.264 (80)	(311)
IrO_2	83.369	82.985	83.380	83.224	83.182 (10)	(321)
Ir	88.054	87.885	87.997	87.951	88.062 (15)	(222)

A.2 Deposition parameters

Table A.2.1 *Standard sputter parameters for TaSiN deposition.*

Gas	99 % Ar + 1 % N_2
Flushing time	600 s
Pre-sputter time	60 s
Substrate temperature	Room temperature

Table A.2.2 *Sputter parameter for deposition of TaSiN with different composition.*

Target, Ta:Si	Composition	Power, [W]	Sputter time, [s]	Thickness, [nm]
1:2.7	$Ta_{15}Si_{44}N_{41}$	120	200	80
	$Ta_{19}Si_{54}N_{26}$	180	200	130
	$Ta_{21}Si_{57}N_{21}$	240	454	330
1:1	$Ta_{22}Si_{22}N_{54}$	120	900	115
	$Ta_{28}Si_{28}N_{43}$	180	700	150
	$Ta_{33}Si_{33}N_{33}$	240	454	160

Table A.2.3 *Standard sputter parameters for platinum deposition.*

Gas	Ar
Flushing time	60 s
Pre-sputter time	10 s
Power	375 W
Sputter time	54 s
Sputter rate	18.5 $Å s^{-1}$
Substrate temperature	Room temperature

Table A.2.4 *DC Sputter parameter for tantalum deposition.*

Gas	Ar
Gas flow	25 sccm
Flushing time	60 s
Pre-sputter time	60 s
Power	150 W
Sputter time	7 s
Sputter rate	6 $Ås^{-1}$
Substrate temperature	Room temperature

Table A.2.5 *DC sputter parameters for iridium deposition.*

Gas	Ar
Gas flow	60 sccm
Flushing time	60 s
Pre-sputter time	10 s
Power	200 W
Sputter time	90 s
Sputter rate	11 $Ås^{-1}$
Substrate temperature	Room temperature

A.3 Nerve cell – basic architecture and electrical excitability

A nerve cell (diameter ranging from 0.2 – 20 μm) is surrounded by a cell membrane (thickness around 8 – 10 nm) with an electrically insulating core of lipid. The cell membrane is a diffusion barrier for hydrophilic substances [25].The phospholipid bilayer (thickness about 5nm) separates the environment (extracellular fluid) from the intracellular fluid. Sodium (Na^+) and chloride (Cl^-) ions are more concentrated outside the cell, and potassium (K^+) ions and organic anions (A^-) are more concentrated in the cell, as depicted in the Figure A.3.1. The ion transport across the cell membrane is possible through i) voltage-gated ion channels, ii) chemically-gated ion cannels, and iii) ion pumps (the ions transport against their concentration gradient). The density of voltage-gated Na^+ and K^+ channels is very high especially on the axon hillock.

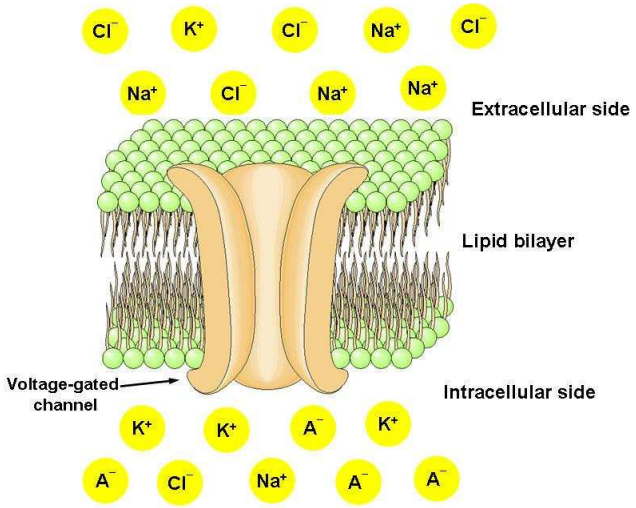


Figure A.3.1 *Cell membrane: the phospholipids from bilayer have hydrophilic head and hydrophobic tail. The hydrophilic heads are oriented to the extracellular and intracellular fluid. The voltage-gated ion channel in the cell membrane is illustrated.*

The different concentrations of the charges inside and outside the cell lead to a difference in electrochemical potential across the membrane (Figure A.3.1). The membrane potential (V_m) is defined as a potential difference of [26]:

$$V_m = V_{in} - V_{out} \tag{A.3.1}$$

the potential inside (V_{in}) and outside (V_{out}) the cell. The membrane potential at a rest is called the resting membrane potential (V_r). It can be in the range between –40 mV and –80 mV. At a rest, a neuron has an excess of negative charges on the inside of the membrane and an excess of positive charges on the outside. The equilibrium potential for any ion X can be calculated from Nernst equation:

$$V_X^0 = \frac{k_B T}{ze} \ln \frac{[X]_o}{[X]_i} \tag{A.3.2}$$

where k_B is the Boltzmann constant, T the temperature, z the valence of the ion, e the elementary charge, $[X]_o$ and $[X]_i$ are the concentrations of the ion outside and inside of the cell, respectively. The equilibrium potentials for some ions are listed in Table A.3.1.

Table A.3.1 *The ion concentration and the equilibrium potential across a neuronal membrane of the squid [24].*

Species of Ion	Concentration in the cell, [mM]	Concentration in extracellular fluid, [mM]	Equilibrium potential, [mV]
K^+	400	20	-75
Na^+	50	440	+55
Cl^-	52	560	-60
A^- (organic)	385	/	/

The transmission of signal or information between neurons is achieved as a combination of chemical and electrical signals. The neuron transmitting a signal is called the presynaptic cell and the one receiving the information is called the postsynaptic cell (Figure A.3.2). The small space between two neurons represents the synaptic cleft. An action potential causes a release of neurotransmitters at the presynaptic terminal into the synaptic cleft. The neurotransmitters bind to the receptor on the postsynaptic neuron generating a local electrical signal, called synaptic potential. In this way the electrical signal is translated into a chemical and again into an electrical one. The synaptic potential can be more positive than the resting potential causing a depolarisation of the membrane (or a hyperpolarisation). When membrane potential at the axon hillock is disturbed to a more positive value, the voltage-gated Na^+ channels open rapid. Na^+ ions move into the cell due to the large electro-chemical gradient, further depolarizing the cell and the cell potential becomes more positive. When a certain threshold value is achieved ($V_m = -55$ mV), a brief voltage pulse is generated, the action potential, that propagates down the length of neuron. The delayed opening of voltage-gated K^+ channels occurs and K^+ ions leave the cell, which leads a recovery of the membrane potential and return to it resting value (repolarisation). The action potential has an all-or-non response: the same amplitude (about 100 mV), duration (about 1.5 ms) and shape [26]. The stimulus duration determines only the number of triggering the action potentials.

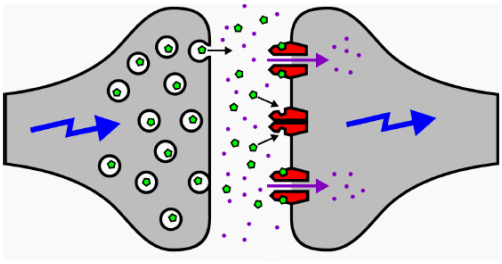


Figure A.3.2 *Communication between neurons: an action potential causes release of neurotransmitters from vesicles. They bind to specific receptors and elicit the opening of the ion channels. The change in membrane potential triggers an action potential which travels down the axon [37].*

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